

Worcester Polytechnic Institute
Department of Electrical and Computer Engineering
ECE3311 Principles of Communication Systems B05
Exercise#6

Envelope detector layout

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- I. Input impedance of the HSMS-285x diode at 0.32 mA bias current
 - II. Changes in Project 5 – vias
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The present project will modify exercise #5 by introducing a more realistic diode detector layout and the DC power supply connections. We will not model the 3D surface-mount bulk components and bond wires precisely, even though it can (and should) be done in a high-quality design in ANSOFT. Instead, we will only model the footprints of the chip diode, chip capacitor, and two RF chokes.

I. Input impedance of the HSMS-285x diode at 0.32 mA bias current

To uniquely define the problem, we will assume that the diode bias current is now 0.32 mA. This corresponds to the resonance condition for the diode itself (the reactance is zero – see exercise #5) at 920 MHz. However, the diode resistance is not exactly 100 Ω but 104 Ω at the resonance. Even though this difference is minor, we will take it into account.

II. Changes in Project 5 – vias

Vias are made with electrically plated holes and they connect the tracks from one size of the board to another. The via (or the plated hole) can only have discrete diameter values – see, for example, Appendix A. Holes in vias are usually smaller than the common low-frequency DIP IC component pads, with 0.5-0.7 mm being typical.

Three vias will be used in this project. The vias are modeled by PEC cylinders. The cylinder can be either open or closed: the effect of metal cap only becomes apparent when frequency wavelength is approaching the via diameter. Since it almost never happens in practice (frequency should be around 500 GHz and FR4 as a material will never work at that frequency) we will use the closed (simpler) PEC cylinders.

1. Rename

Save ANSOFT Project 5 as Project 6

2. Remove the obsolete ground connection

Disconnect the 100 Ω lumped load from the ground plane (delete the PEC connector to ground plane).

3. Via for capacitor

Insert via – a PEC cylinder that will connect capacitor to ground:

Command	CreateCylinder			
Coordinate System	Global			
Center Position	30.83 ,5.85 ,-0.79	mm	30.83mm , -5.85mm , -0...	
Axis	Z			
Radius	0.32	mm	0.32mm	
Height	1.58	mm	1.58mm	

4. Vias for DC power supply

Insert two other vias – two PEC cylinders that will connect the DC power supply:

Command	CreateCylinder			
Coordinate System	Global			
Center Position	22.7 ,29.2 ,-0.79	mm	22.7mm , 29.2mm , -0.7...	
Axis	Z			
Radius	0.32	mm	0.32mm	
Height	1.58	mm	1.58mm	
Command	CreateCylinder			
Coordinate System	Global			
Center Position	32.7 ,29.2 ,-0.79	mm	32.7mm , 29.2mm , -0.7...	
Axis	Z			
Radius	0.32	mm	0.32mm	
Height	1.58	mm	1.58mm	

III. Changes in diode/capacitor/resistor layout

1. Diode footprint

Replace the lumped load resistance to $104\ \Omega$. The rectangle corresponding to the lumped load (1.27x1.52 mm) will now model the diode footprint only. According to Appendix A we should be able to properly position the diode SOT-23 package in place of this imaginary rectangle.

2. Connection to protoboard

Connect the diode to the opposite side of the board using a “low-impedance” – wide¹ microstrip – a PEC rectangle:

Command	CreateRectangle			
Coordinate System	Global			
Position	29.05 ,2.54 ,0.79	mm	29.05mm , -2.54mm , 0....	
Axis	Z			
XSize	19.21	mm	19.21mm	
YSize	5.08	mm	5.08mm	

3. Capacitor footprint

Insert a new RLC rectangle (1.27x1.52 mm) that will model the 100 pF capacitor footprint – see Appendix A.

Command	CreateRectangle			
Coordinate System	Global			
Position	30.32 ,-4.06 ,0.79	mm	30.32mm , -4.06mm , 0....	
Axis	Z			
XSize	1.27	mm	1.27mm	
YSize	1.52	mm	1.52mm	

According to Appendix A we should be able to properly position the chip capacitor (Panasonic) in place of this imaginary rectangle. Assign 100 pF lumped RLC load to that rectangle.

4. Capacitor plating

Insert a new PEC rectangle (3.56x3.56 mm) that will model another part of capacitor connection to ground:

¹ Note: a wide microstrip has a low characteristic impedance whereas a very narrow microstrip has a high impedance. Therefore, narrow microstrips are typically used to connect the DC bias power to an RF circuit.

Command	CreateRectangle			
Coordinate System	Global			
Position	29.05 ,-7.62 ,0.79	mm	29.05mm , -7.62mm , 0....	
Axis	Z			
XSize	3.56	mm	3.56mm	
YSize	3.56	mm	3.56mm	

5. Protoboard load

The 100 k Ω resistor of the envelope detector belongs to the “baseband” part of the circuit. This resistor can in fact be the input resistance of the low-frequency baseband amplifier for AM modulation $m(t)$. Therefore, we will not put a separate chip resistor on the board. Instead, a 100 k Ω termination to ground (100 k Ω RLC boundary) is introduced as follows:

Command	CreateRectangle			
Coordinate System	Global			
Position	96.52/2 ,-2.54 ,-0.79	mm	48.26mm , -2.54mm , -0...	
Axis	X			
YSize	5.08	mm	5.08mm	
ZSize	1.58	mm	1.58mm	

IV. DC power connections

1. DC power traces

Two narrow PEC power traces (+/-) are introduced first:

Command	CreateRectangle			
Coordinate System	Global			
Position	20.16 ,0.76 ,0.79	mm	20.16mm , 0.76mm , 0....	
Axis	Z			
XSize	0.254	mm	0.254mm	
YSize	25.4	mm	25.4mm	
Command	CreateRectangle			
Coordinate System	Global			
Position	30.16 ,0.76+1.78 ,0.79	mm	30.16mm , 2.54mm , 0....	
Axis	Z			
XSize	0.254	mm	0.254mm	
YSize	25.4-1.78	mm	23.62mm	

2. Footprints for RF chokes

Footprints for two 39 nH Murata RF chokes (see Appendix A) are introduced next, using two RLC boundaries (39 nH each):

Command	CreateRectangle			
Coordinate System	Global			
Position	20.16 ,26.16 ,0.79	mm	20.16mm , 26.16mm , 0...	
Axis	Z			
XSize	0.254	mm	0.254mm	
YSize	0.51	mm	0.51mm	
Command	CreateRectangle			
Coordinate System	Global			
Position	30.16 ,26.16 ,0.79	mm	30.16mm , 26.16mm , 0...	
Axis	Z			
XSize	0.254	mm	0.254mm	
YSize	0.51	mm	0.51mm	

You may want to use the “red” magnifier  in order to fit these very small rectangles in the active window (after selection).

3. Via plates

Introduce two PEC rectangles for either power connection (copy and paste rectangles for simplicity):

Command	CreateRectangle			
Coordinate System	Global			
Position	20.16 ,26.67 ,0.79	mm	20.16mm , 26.67mm , 0...	
Axis	Z			
XSize	5.08	mm	5.08mm	
YSize	5.08	mm	5.08mm	
Command	CreateRectangle			
Coordinate System	Global			
Position	30.16 ,26.67 ,0.79	mm	30.16mm , 26.67mm , 0...	
Axis	Z			
XSize	5.08	mm	5.08mm	
YSize	5.08	mm	5.08mm	

The geometry layout is complete. It is shown for reference purposes in Fig. 1. There should be total 5 RLC boundaries; 12 PEC boundaries, 1 radiation boundary, and one lumped port. The validation check should indicate 5 intersecting PEC boundaries (!): the vias are in contact with either the top traces or with the ground plane.

Basically, in ANSOFT one may unite (Boolean operation) the PEC conductors that are in contact to each other. This operation confirms that there is no narrow gap between the conductors. Such a gap may have been overlooked during geometry operations. The gap may also have a very severe influence on the solution.

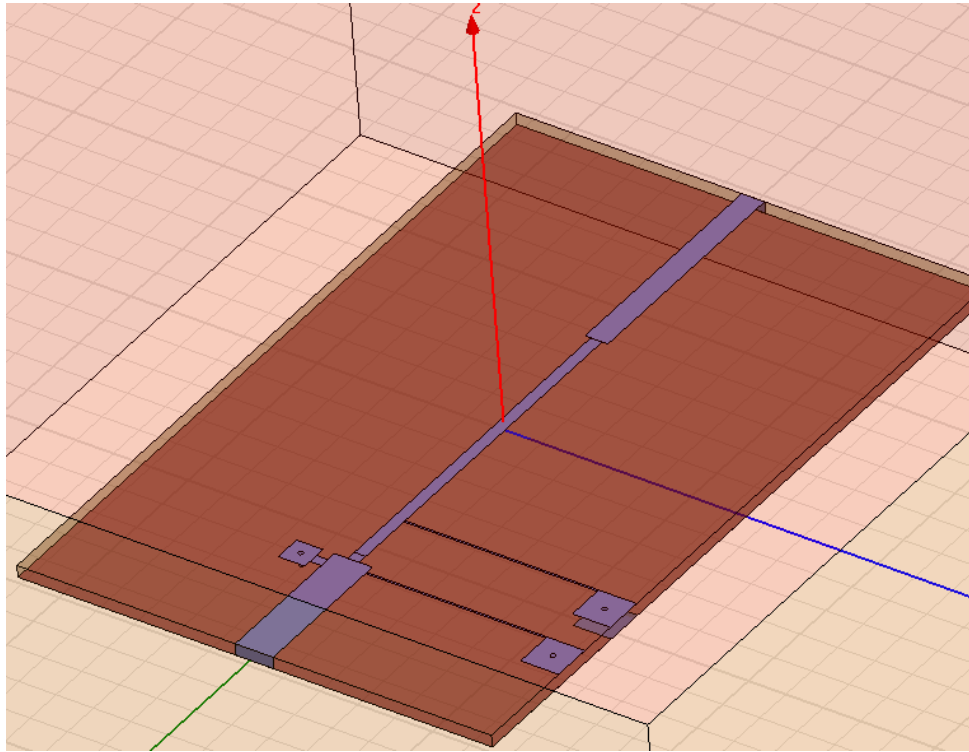


Fig. 1. Geometry layout of the envelope detector.

4. Solution/sweep/output settings

The same as in Project 5. Do not change.

V. Calculation and report

Task 1:

- Plot the geometry layout for your circuit.
- Calculate and plot return loss to diode detector in the frequency range between 900 and 940 MHz. Mark the value at 920 MHz. Is the detector performance better or worse than in exercise #5? How can you explain the difference?
- In order to exactly identify one reason for circuit performance degradation you may want to examine the surface current distribution on all top traces – select all of them simultaneously (while holding Ctrl key) and plot the current magnitude (HFSS/Fields/Fields/J/Mag_Jsurf). Now, should RF current really flow through DC power buses? But what happens in reality? How can you possibly fix the RF “leakage”? This question may be important for this and other circuits.

Next, it is suggested to vary the length of the quarter-wave transformer line to fine tune the circuit. In order to do so, go to “Optimetrics” menu and “Add” a parameter sweep as shown in the figure below. The parameter to vary will be the length parameter e introduced yet in exercise #5.

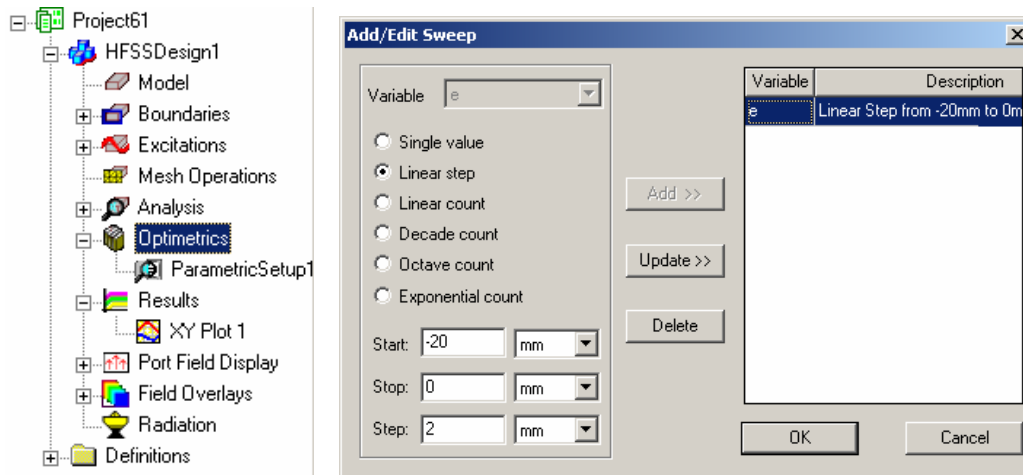
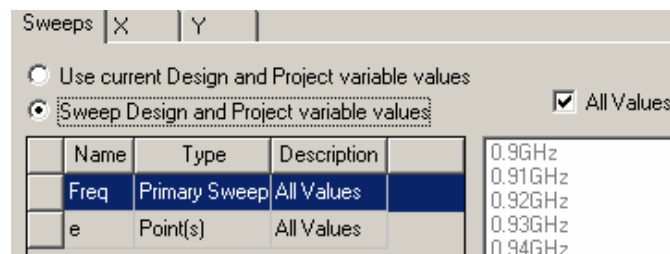


Fig. 2. Introducing parametric sweep into the project.

Task 2:

- Run parametric sweep – may be a lengthy task!
- When plotting the results for return loss go to “Sweeps” menu and turn on option “Sweep Design and Project variable values” as shown below:

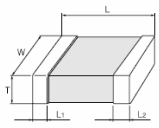
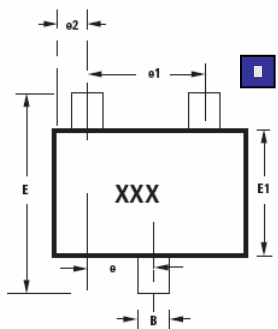
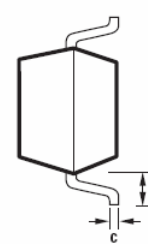
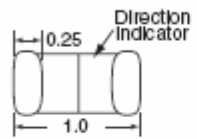


This will give return loss for every value of the length parameter e on the same plot.

- From the plot of return loss to diode detector, could you possibly identify the best value of parameter e ? Note that it should be rather the “safest” value, where a small variation around it does not lead to a large “jump” in return loss. To better resolve the problem you may want to change/refine and rerun the parametric sweep.

1. A report to exercise#6 should address tasks 1 and 2 listed in this section.
2. The report is to be prepared and submitted **separately** from HW#5. Due: Friday, together with HW#5.

Appendix A Detector components

Component	Vendor	DigiKey part number	Size																																													
Capacitor 100 pF	Panasonic - ECG ECJ-2VC1H101J	PCC101CGCT-ND	2×1.25 mm ■ Dimensions in mm (not to scale)  <table><thead><tr><th>Code</th><th>Size Code (EIA)</th><th>L</th><th>W</th><th>T</th><th>L1, L2</th></tr></thead><tbody><tr><td>Z</td><td>Type "06" (0201)</td><td>0.60±0.03</td><td>0.30±0.03</td><td>0.30±0.03</td><td>0.15±0.05</td></tr><tr><td>0</td><td>Type "10" (0402)</td><td>1.00±0.05</td><td>0.50±0.05</td><td>0.50±0.05</td><td>0.2±0.1</td></tr><tr><td>1</td><td>Type "11" (0603)</td><td>1.6±0.1</td><td>0.8±0.1</td><td>0.8±0.1</td><td>0.3±0.2</td></tr><tr><td rowspan="4">2</td><td rowspan="4">Type "12" (0805)</td><td>2.0±0.1</td><td>1.25±0.10</td><td>0.6±0.1</td><td rowspan="4">0.50±0.25</td></tr><tr><td></td><td></td><td>0.85±0.10</td></tr><tr><td></td><td></td><td>1.25±0.10</td></tr><tr><td>2.00±0.15</td><td>1.25±0.15</td><td>1.25±0.15</td></tr><tr><td></td><td></td><td>2.0±0.2</td><td>1.25±0.20</td><td>1.25±0.20</td><td></td></tr></tbody></table> Unit : mm	Code	Size Code (EIA)	L	W	T	L1, L2	Z	Type "06" (0201)	0.60±0.03	0.30±0.03	0.30±0.03	0.15±0.05	0	Type "10" (0402)	1.00±0.05	0.50±0.05	0.50±0.05	0.2±0.1	1	Type "11" (0603)	1.6±0.1	0.8±0.1	0.8±0.1	0.3±0.2	2	Type "12" (0805)	2.0±0.1	1.25±0.10	0.6±0.1	0.50±0.25			0.85±0.10			1.25±0.10	2.00±0.15	1.25±0.15	1.25±0.15			2.0±0.2	1.25±0.20	1.25±0.20	
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Schottky Diode	Agilent HSMS-2850-TR1 SOT-23	HSMS-2850-TR1-ND	Package Dimensions Outline 23 (SOT-23)   <table><thead><tr><th rowspan="2">SYMBOL</th><th colspan="2">DIMENSIONS (mm)</th></tr><tr><th>MIN.</th><th>MAX.</th></tr></thead><tbody><tr><td>A</td><td>0.79</td><td>1.20</td></tr><tr><td>A1</td><td>0.000</td><td>0.100</td></tr><tr><td>B</td><td>0.37</td><td>0.54</td></tr><tr><td>C</td><td>0.086</td><td>0.152</td></tr><tr><td>D</td><td>2.73</td><td>3.13</td></tr><tr><td>E</td><td>1.15</td><td>1.50</td></tr><tr><td>e</td><td>0.89</td><td>1.02</td></tr><tr><td>e1</td><td>1.78</td><td>2.04</td></tr><tr><td>e2</td><td>0.45</td><td>0.60</td></tr><tr><td>E</td><td>2.10</td><td>2.70</td></tr><tr><td>L</td><td>0.45</td><td>0.69</td></tr></tbody></table> Notes: XXX - package marking Drawings are not to scale 	SYMBOL	DIMENSIONS (mm)		MIN.	MAX.	A	0.79	1.20	A1	0.000	0.100	B	0.37	0.54	C	0.086	0.152	D	2.73	3.13	E	1.15	1.50	e	0.89	1.02	e1	1.78	2.04	e2	0.45	0.60	E	2.10	2.70	L	0.45	0.69							
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RF choke 39 nH SRF = 1200 MHz	Murata LQG15HS39NJ02D	490-2630-1-ND	LQG15HS Series   Chip inductors specifically designed for high frequency applications. They are designed to realize stable characteristics in high frequency range applying integrated multilayer process. Integrated multilayer process enables a wide range of inductance values with tight tolerance.																																													
Board	Mini board from EXPRESS PCB \$51 for three boards		Board size must be 3.8 x 2.5 inches Our laminate is 0.062" FR-4 epoxy glass with 1/2 ounce copper. No copper (pads or traces) can be placed closer than 0.025" to the perimeter of the board.																																													

			Etching resolution is: 0.007" minimum trace width, 0.007" minimum space width. Fifteen hole sizes are available: 0.020", 0.025", 0.029", 0.035", 0.040", 0.046", 0.052", 0.061", 0.067", 0.079", 0.093", 0.110", 0.125", 0.150", 0.192". These sizes are the finished hole diameters after plating. The dielectric constant of our FR-4 laminate ranges from 4.2 to 5.0.
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