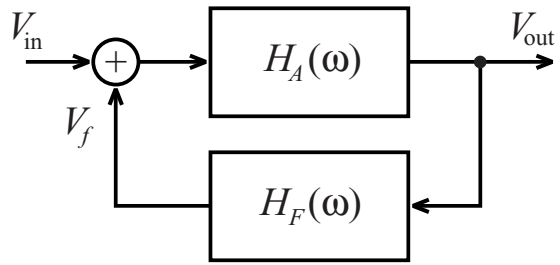
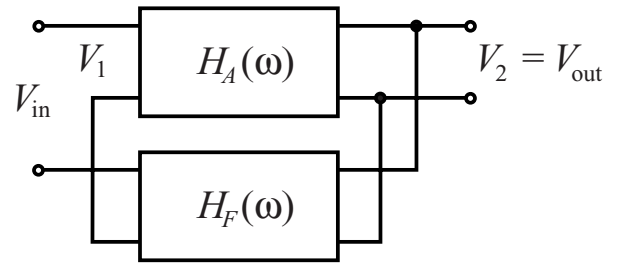


FIGURES FOR CHAPTER 10



(a) Closed-loop circuit model



(b) Network representation

Figure 10-1 Basic oscillator configuration.

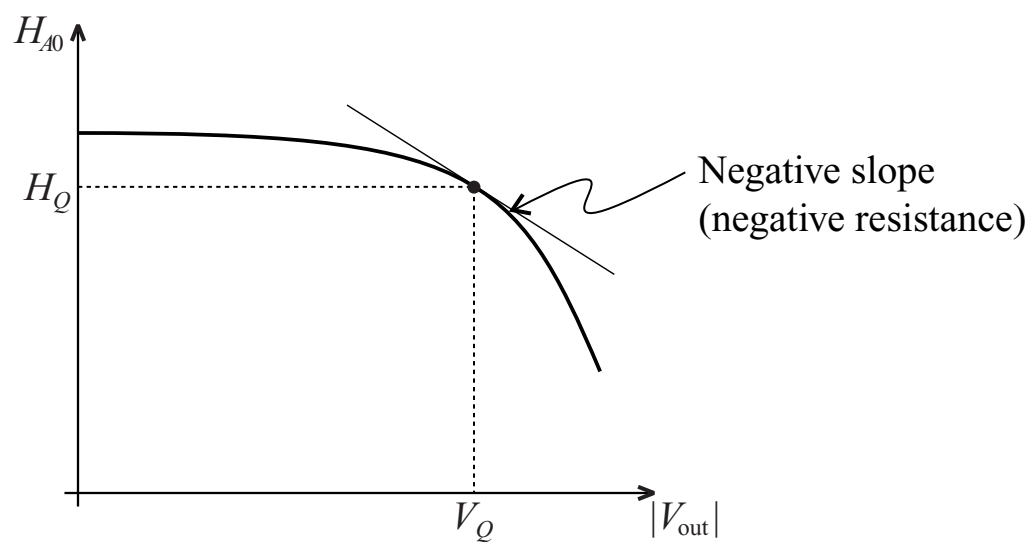


Figure 10-2 Output voltage versus gain characteristic.

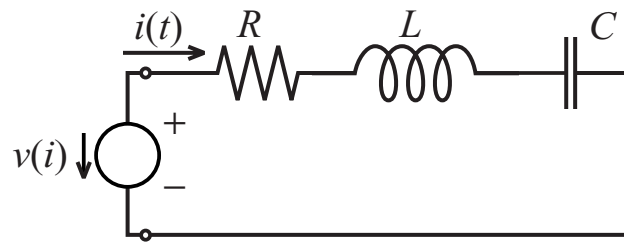
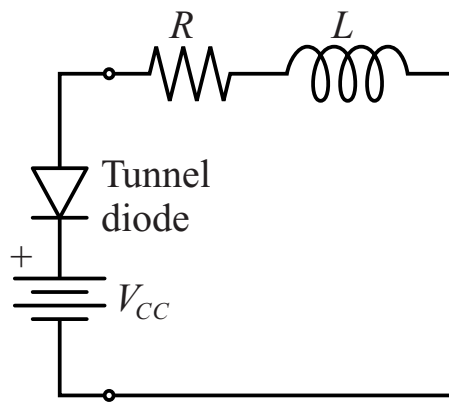
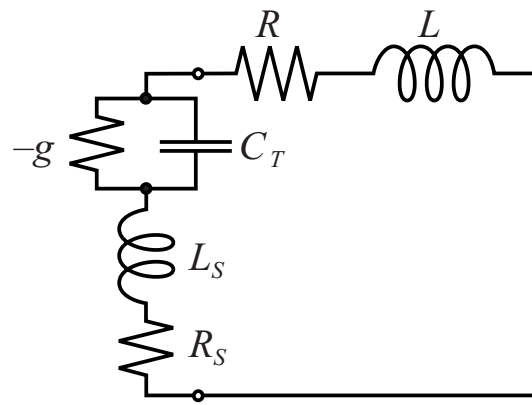


Figure 10-3 Series resonance circuit with voltage-controlled source term.



(a) Tunnel diode oscillator circuit



(b) Small-signal equivalent circuit

Figure 10-4 Tunnel diode oscillator circuit and its small-signal model.

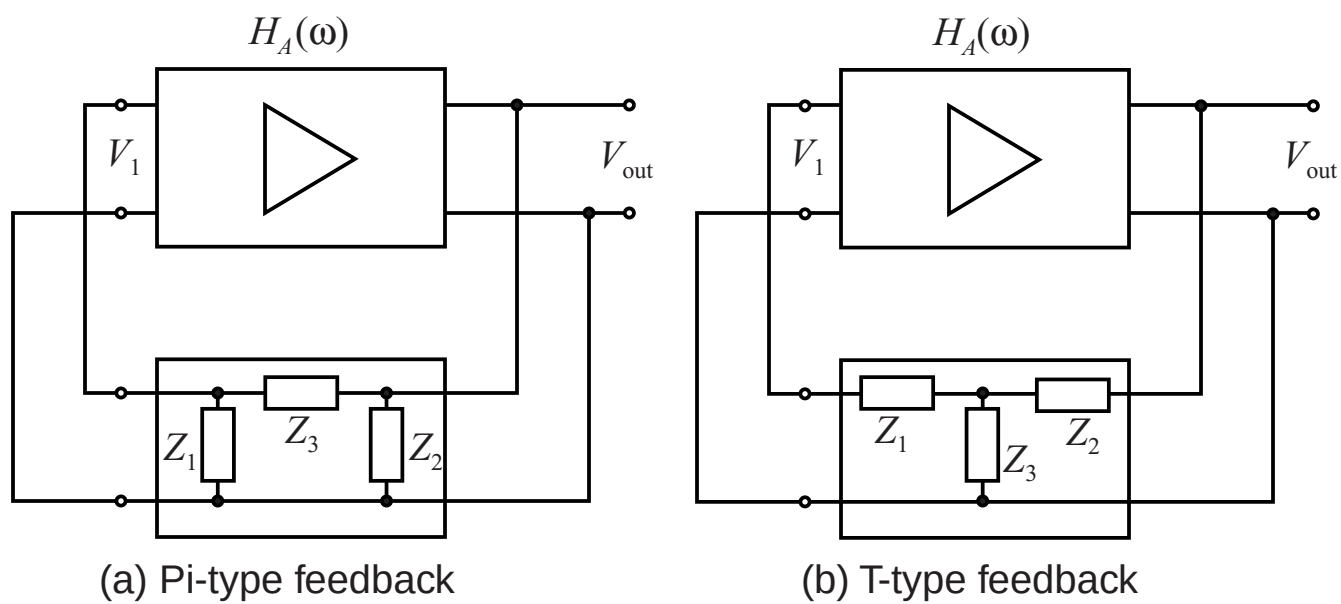


Figure 10-5 Feedback circuits with Pi- and T-type feedback loops.

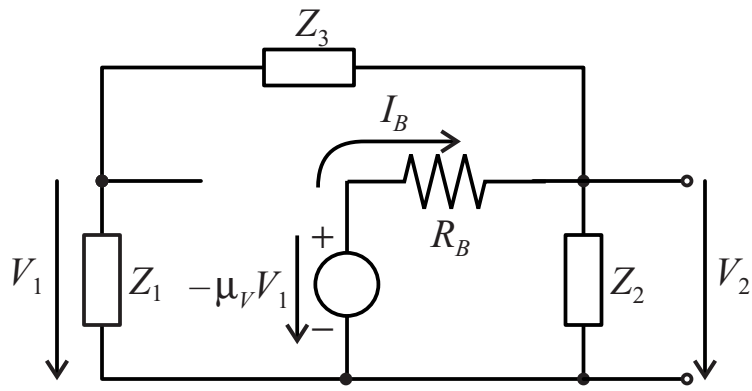
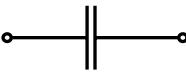
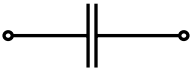
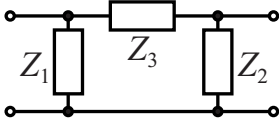
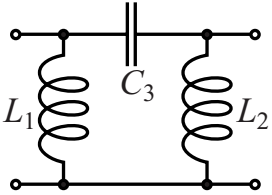
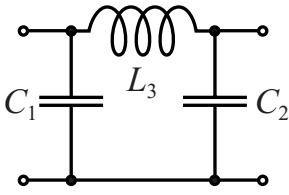
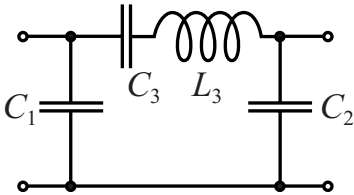
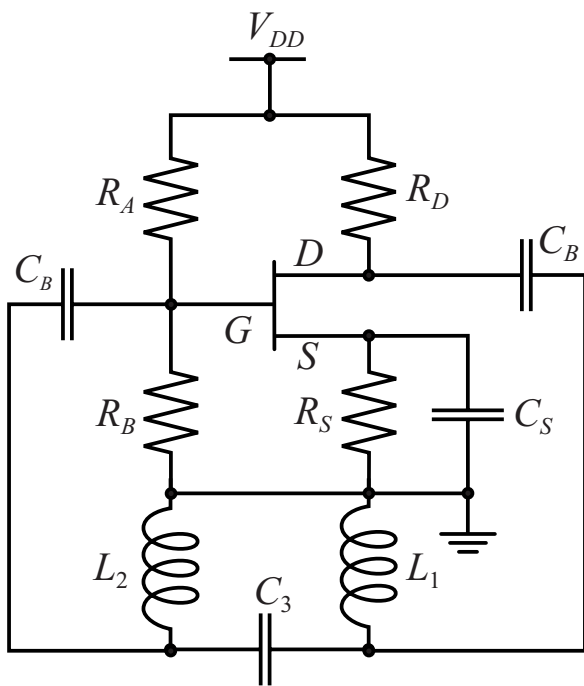


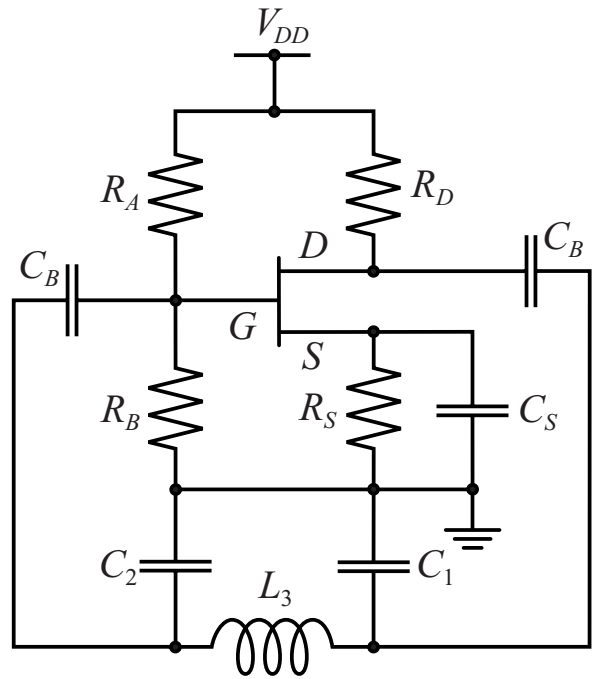
Figure 10-6 Feedback oscillator with FET electric circuit model.

Table 10-1 Various feedback configurations for oscillator designs based on Figure 10-5(a)

X_1, X_2		
X_3		
	 Hartley	 Colpitts  Clapp

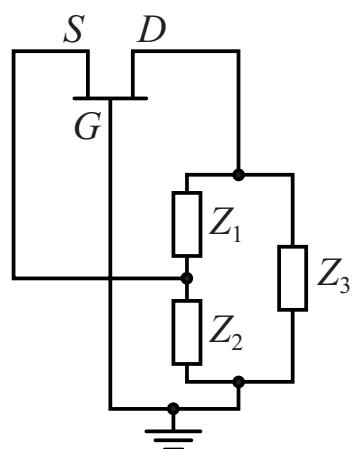


(a) Hartley oscillator

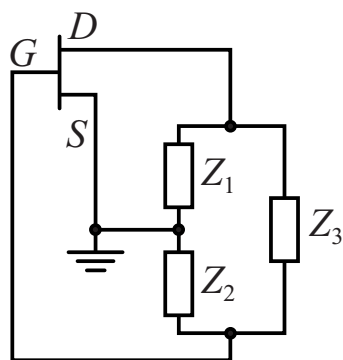


(b) Colpitts oscillator

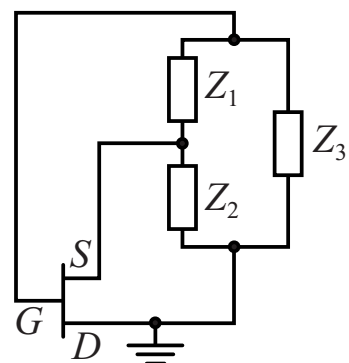
Figure 10-7 Hartley and Colpitts oscillators.



(a) Common gate



(b) Common source



(c) Common drain

Figure 10-8 Common gate, source, and drain configurations.

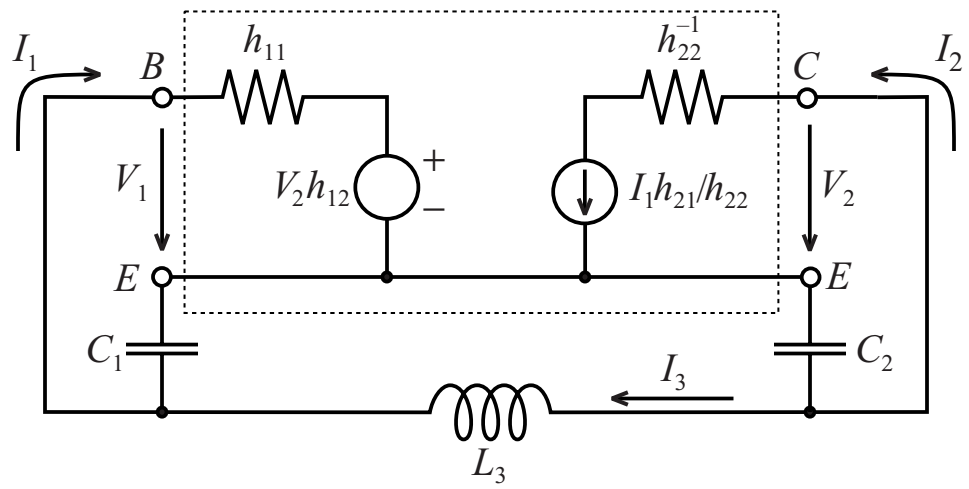


Figure 10-9 Colpitts oscillator design.

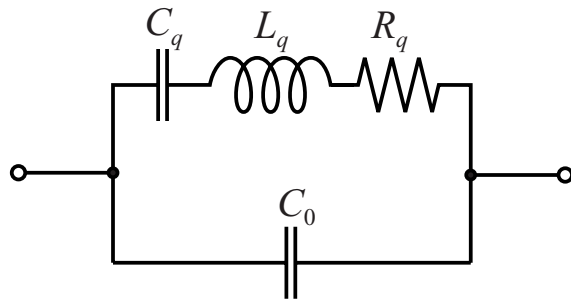


Figure 10-10 Quartz-resonator equivalent electric circuit representation.

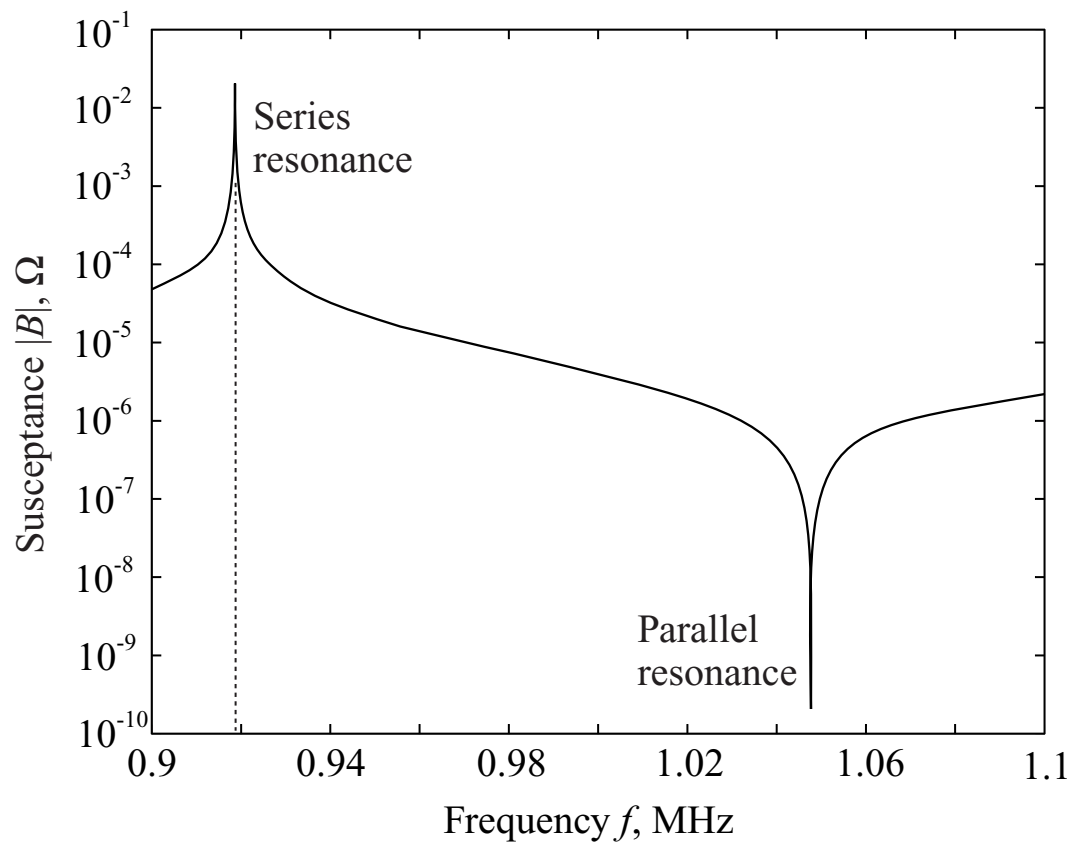
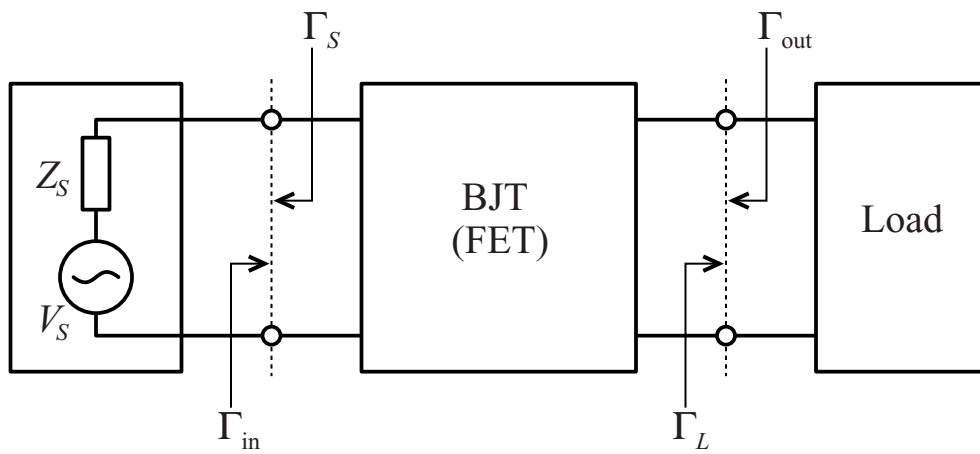
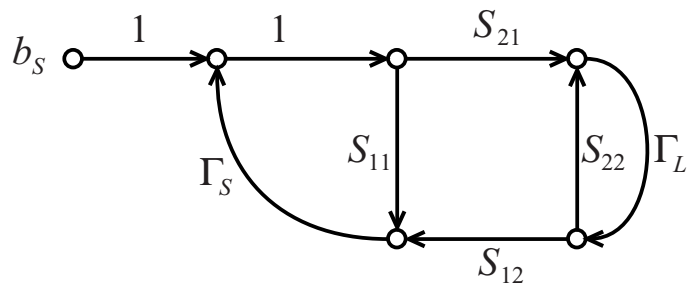


Figure 10-11 Susceptance response of a quartz element.



(a) Sourced and loaded transistor



(b) Equivalent signal flow graph

Figure 10-12 Sourced and loaded transistor and its flow chart model.

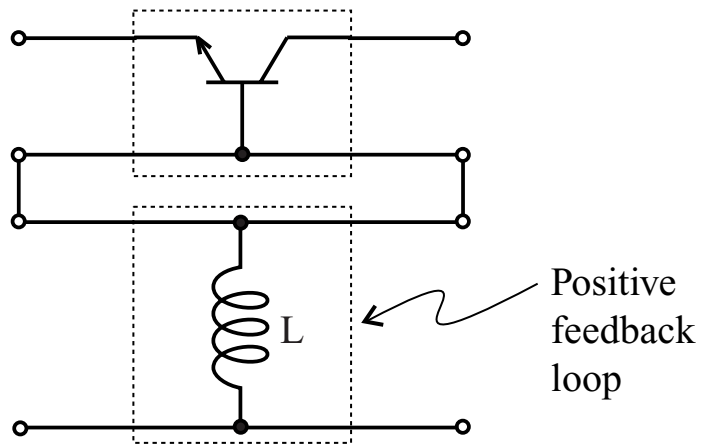


Figure 10-13 Network representation of the BJT with base inductance.

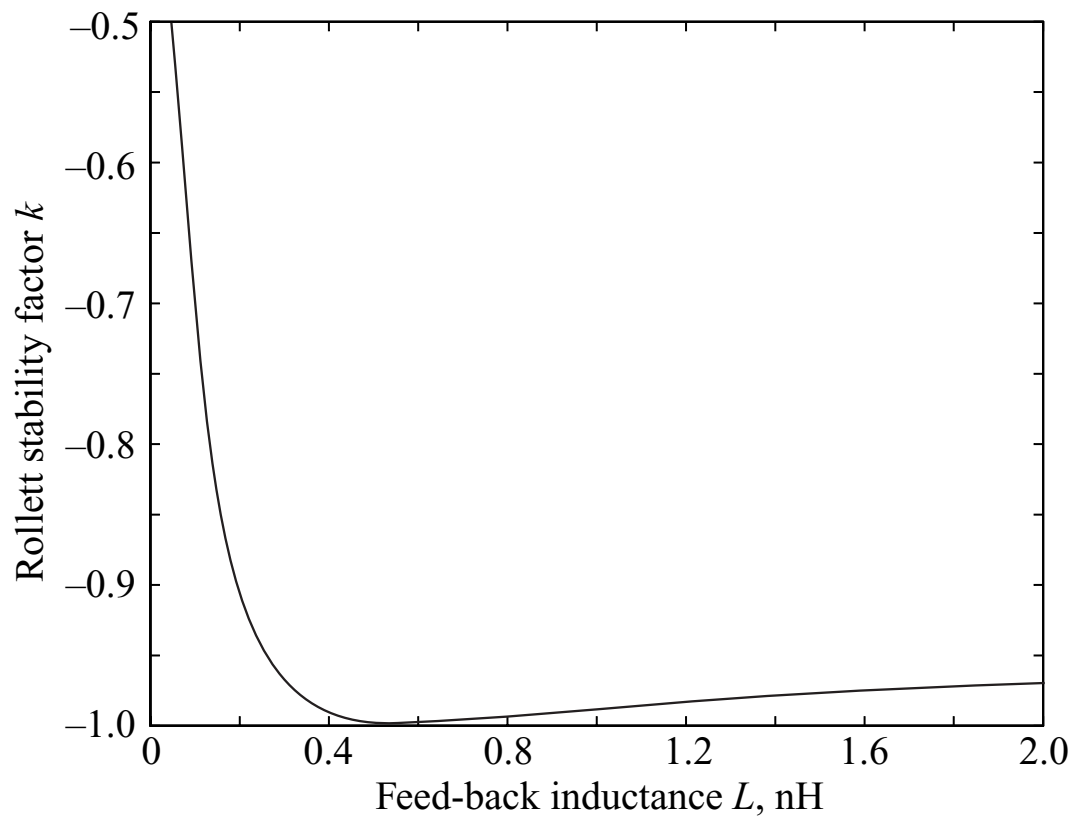


Figure 10-14 Rollett stability factor (k) as a function of feedback inductance in common-base configuration.

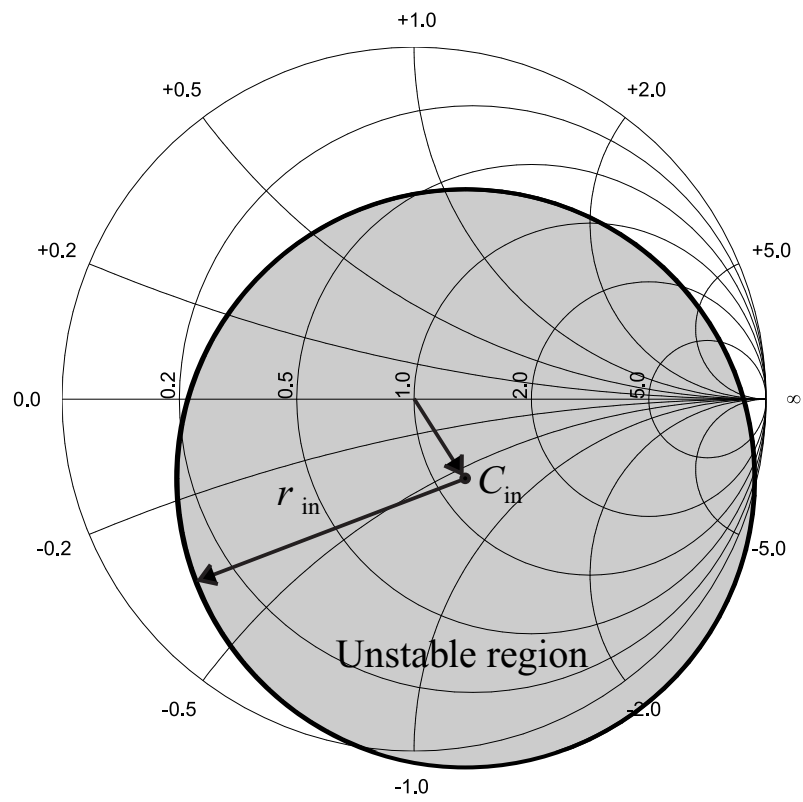


Figure 10-15 Input stability circle for the oscillator design.

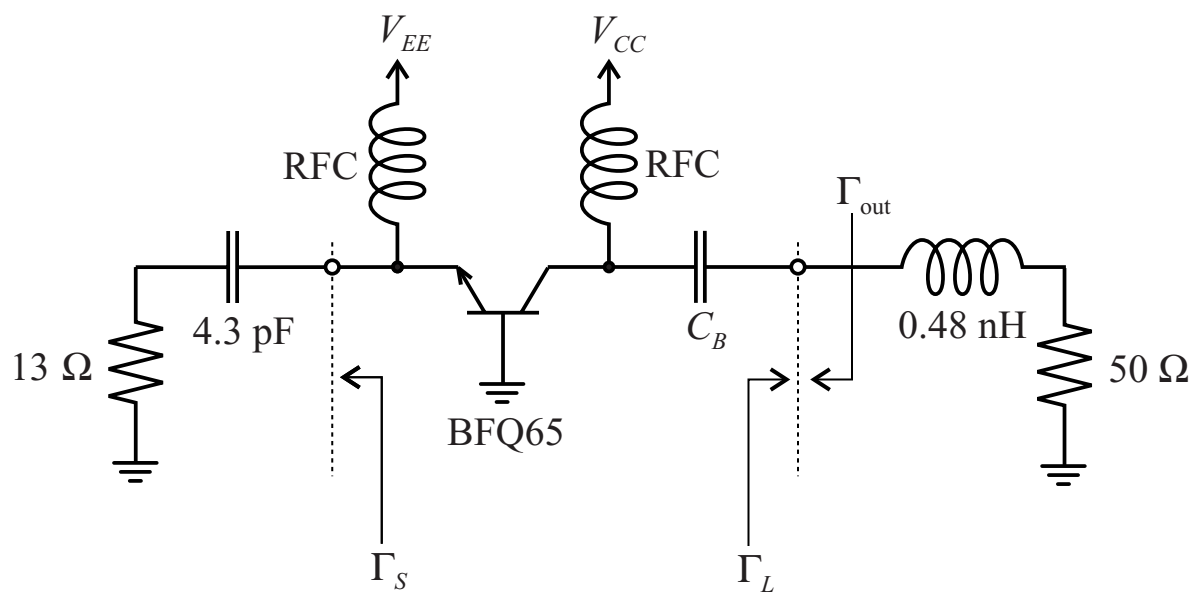


Figure 10-16 Series-feedback BJT oscillator circuit.

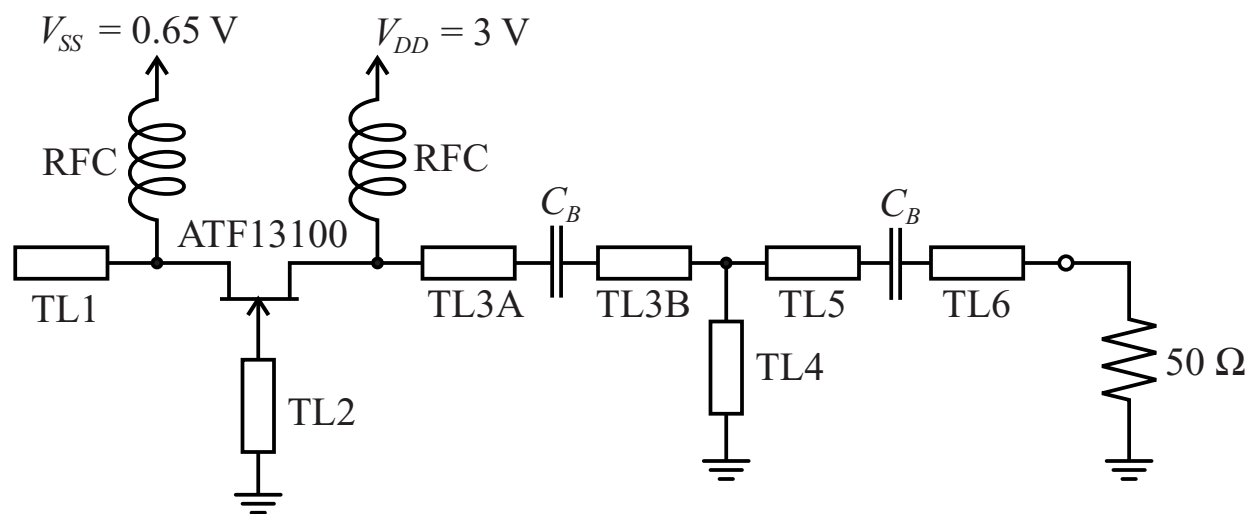


Figure 10-17 GaAs FET oscillator implementation with microstrip lines.

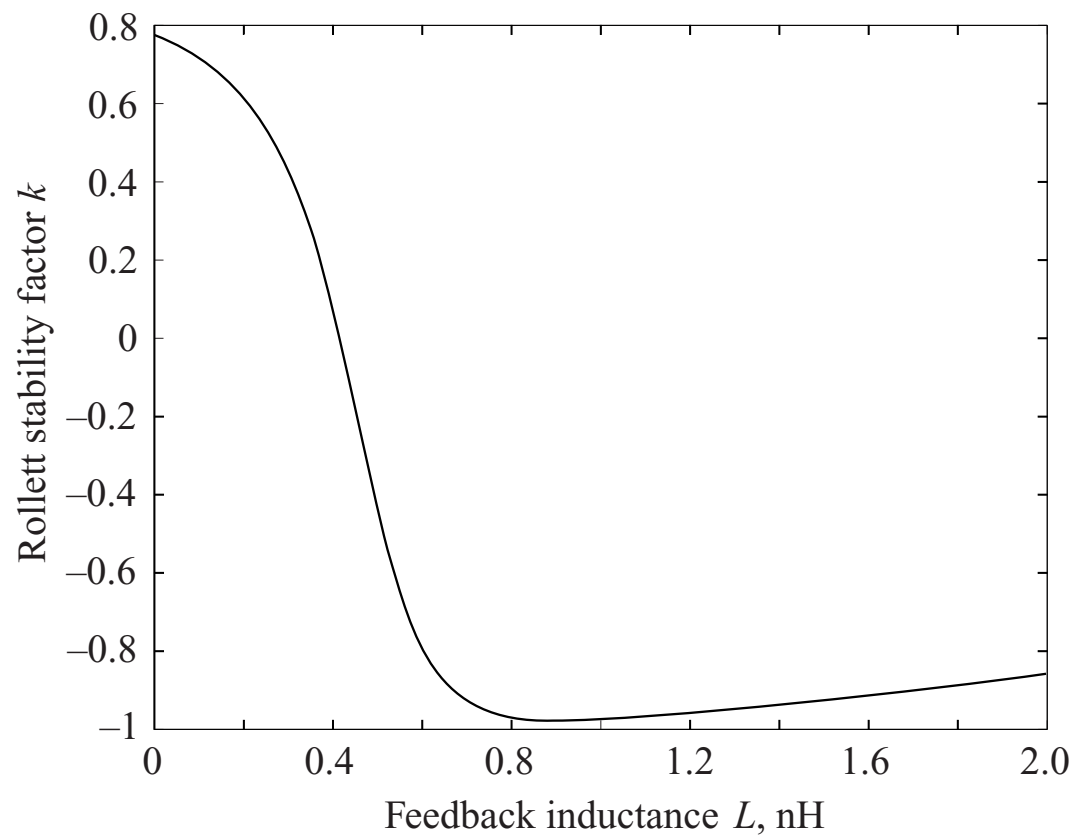


Figure 10-18 Stability factor for FET in common-gate mode as a function of gate inductance.

Table 10-2 Dimensions of the transmission lines in the FET oscillator

Transmission line	Electrical length, deg.	Width, mil	Length, mil
TL1	80	74	141
TL2	48.5	74	86
TL3	67	74	118
TL4	66	74	116

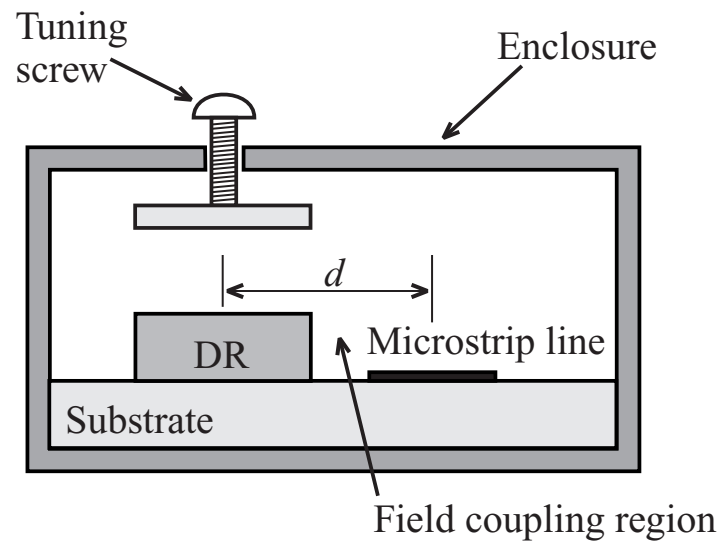
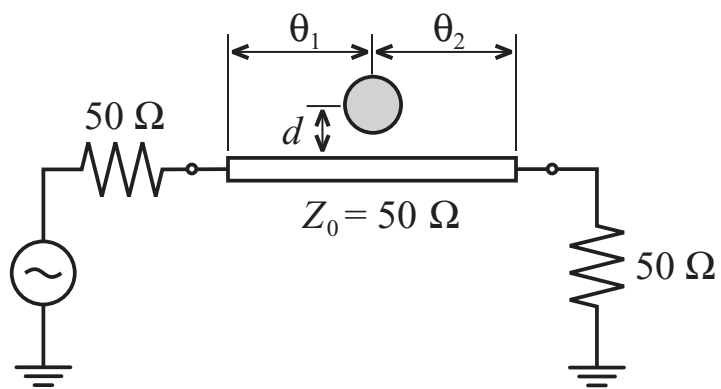
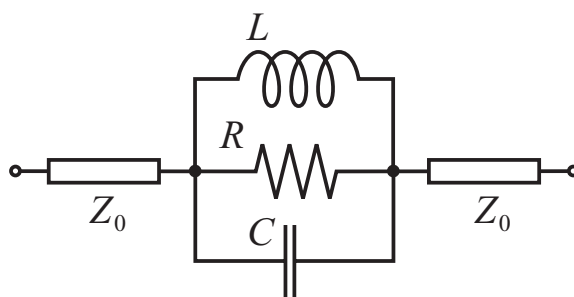


Figure 10-19 Dielectric resonator (DR) placed in proximity to a microstrip line.



(a) Terminated microstrip line with DR



(b) Transmission line model

Figure 10-20 Placement of DR along a transmission line and equivalent circuit representation for S -parameter computation.

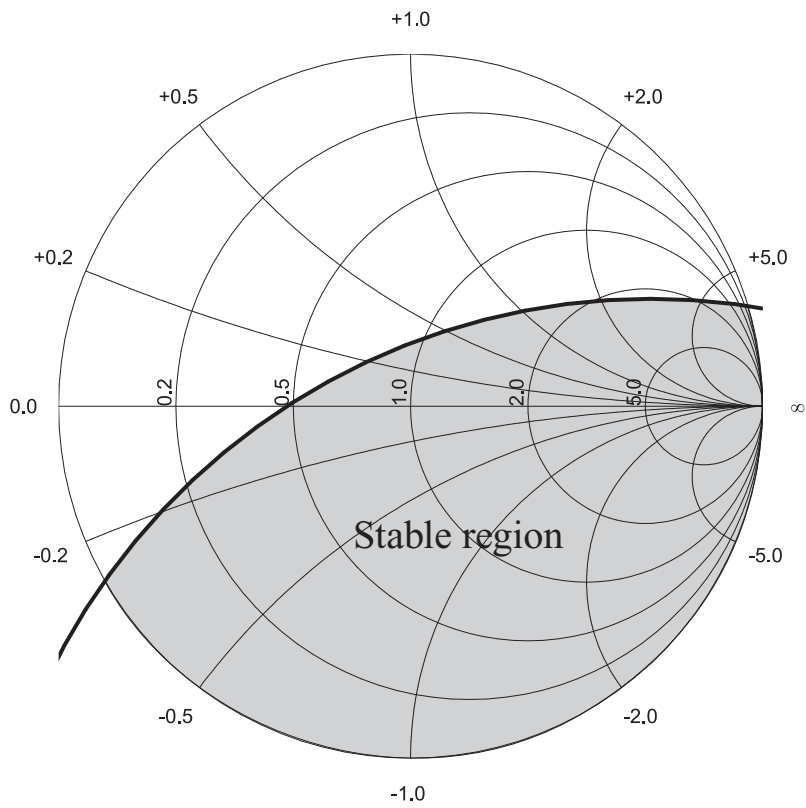


Figure 10-21 Input stability circle of the FET in the DRO design example.

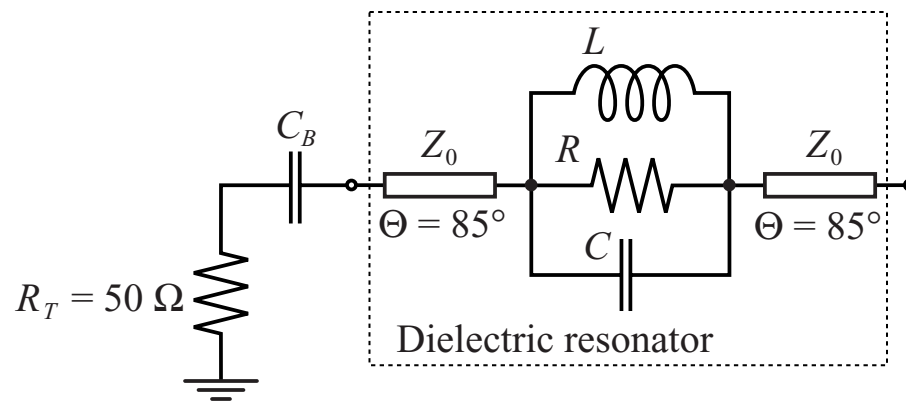
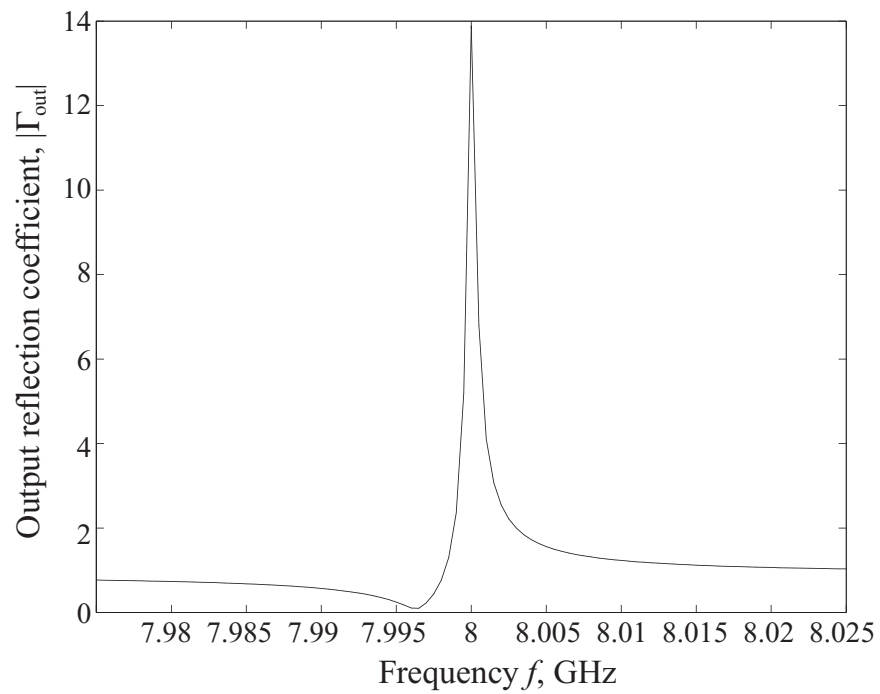
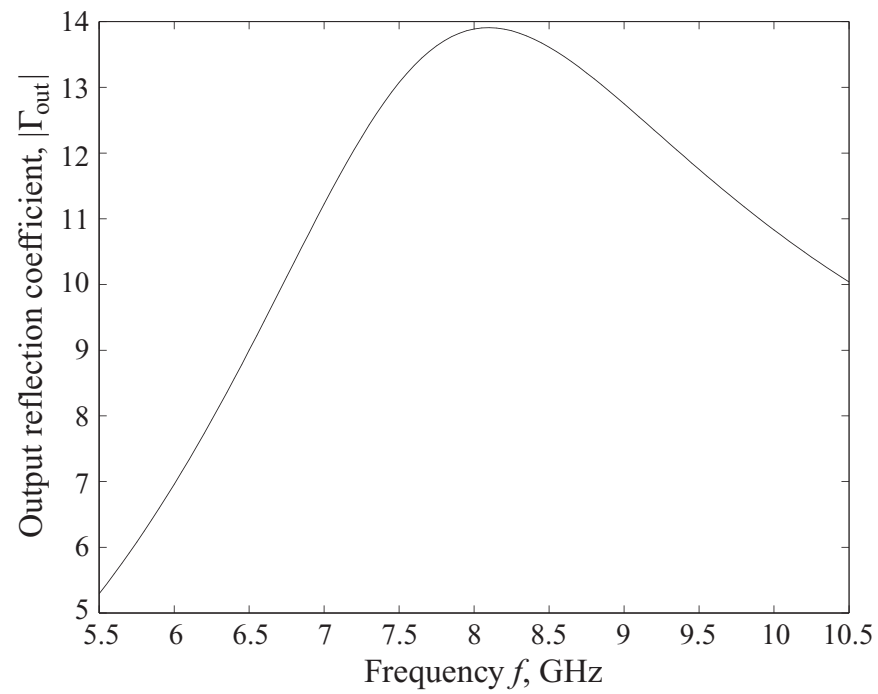


Figure 10-22 DR-based input matching network of the FET oscillator.



(a) Oscillator design with DR



(b) Conventional oscillator without DR

Figure 10-23 Frequency response of the output reflection coefficient for an oscillator design with and without DR.

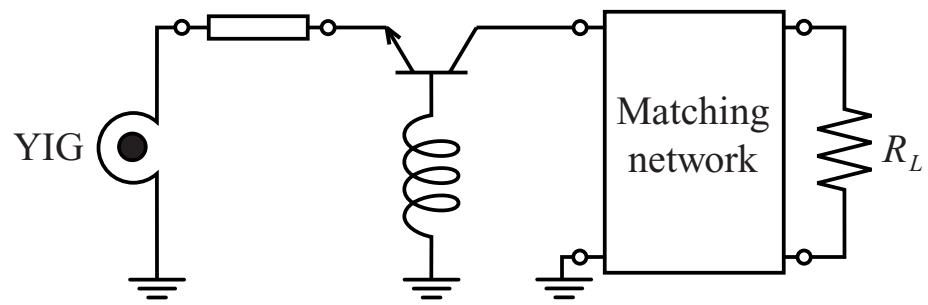


Figure 10-24 Oscillator design based on a YIG tuning element.

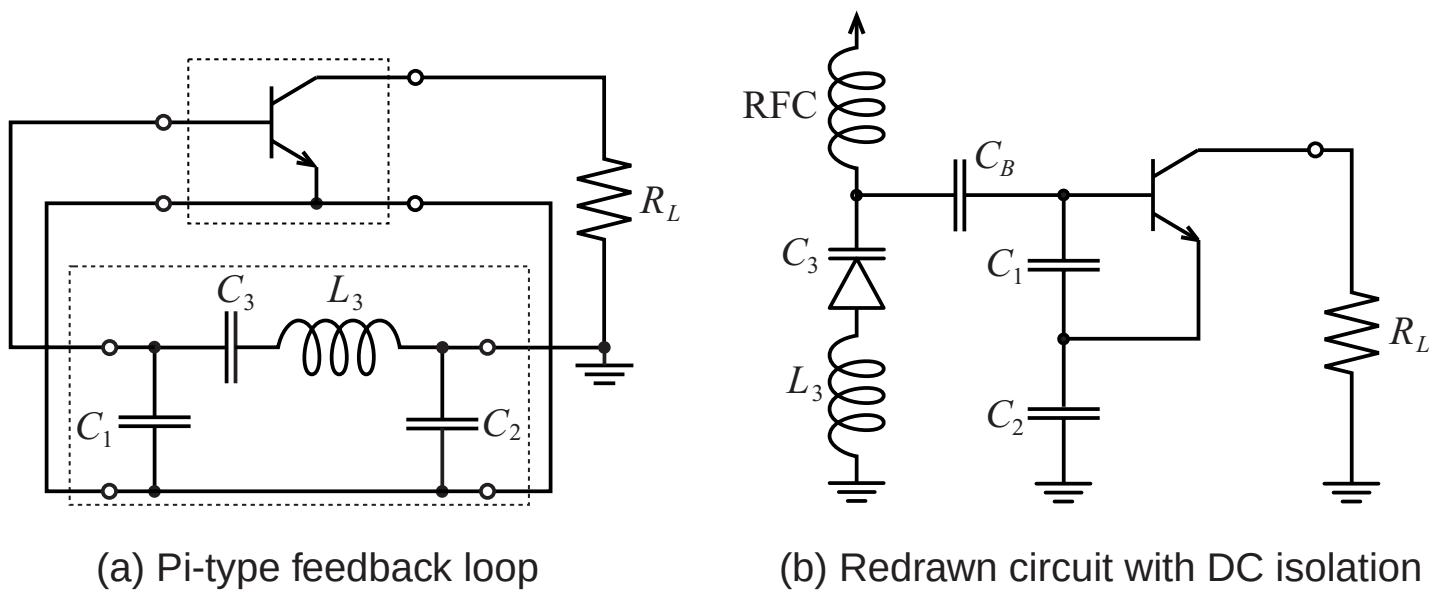


Figure 10-25 Varactor diode oscillator.

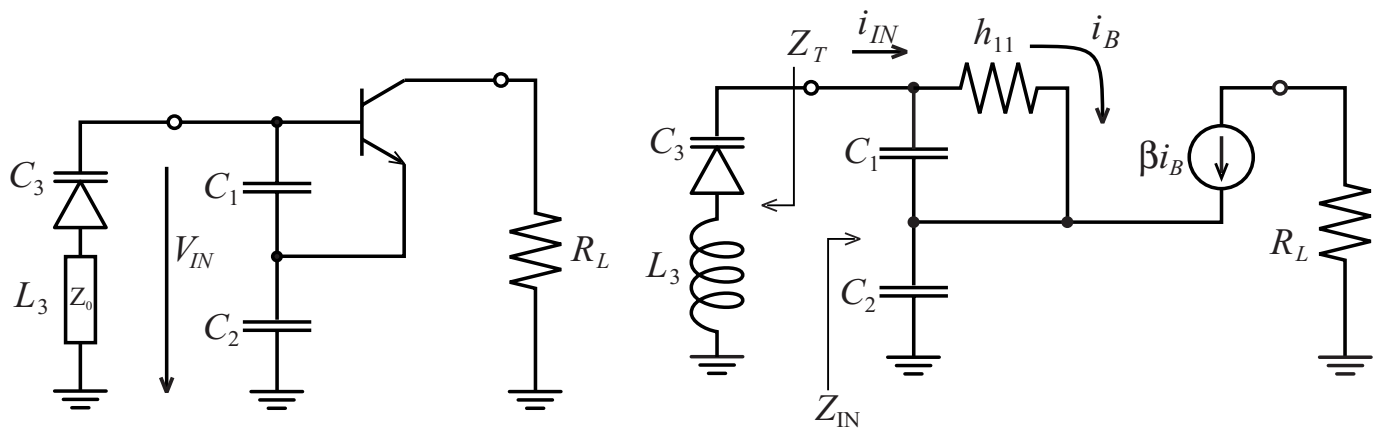
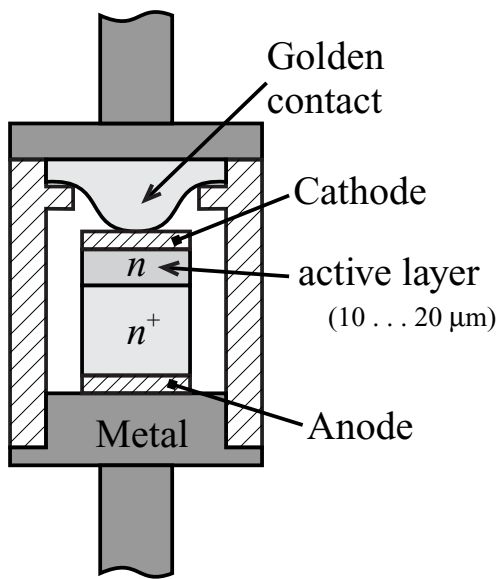
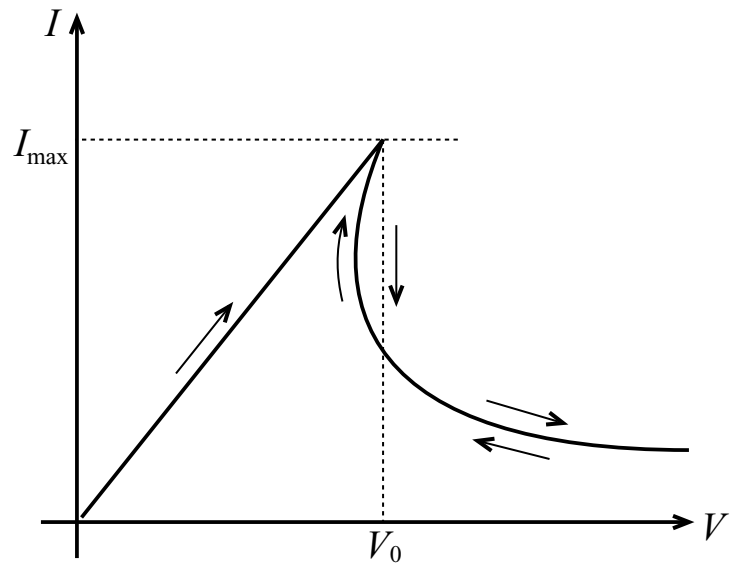


Figure 10-26 Circuit analysis of varactor diode oscillator.



(a) Gunn element structure



(b) Current vs. applied voltage response

Figure 10-27 Gunn element and current versus voltage response.

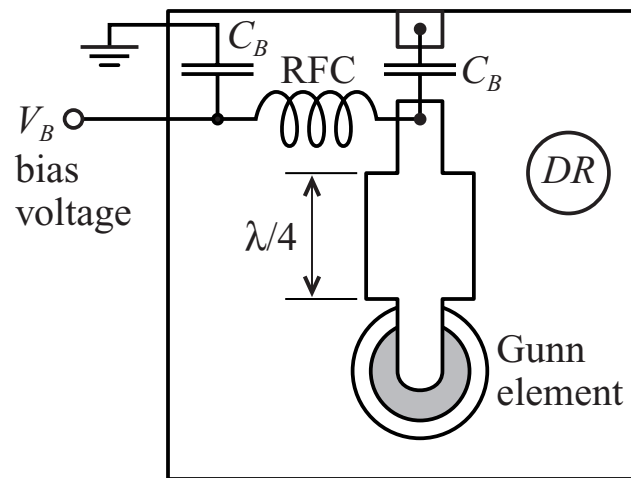


Figure 10-28 Gunn element oscillator circuit with dielectric resonator (DR).

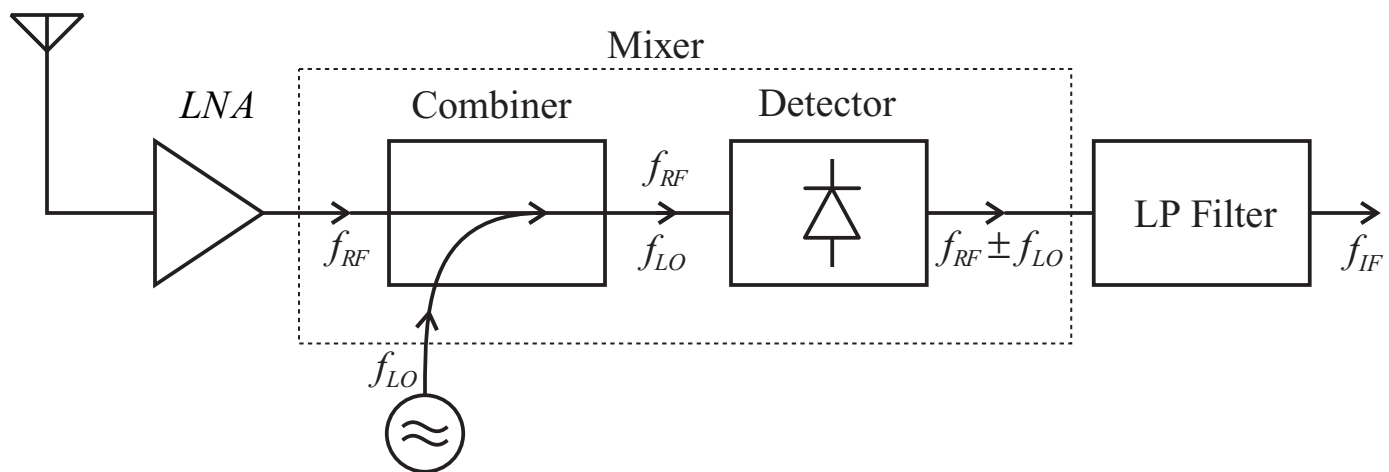


Figure 10-29 Heterodyne receiver system incorporating a mixer.

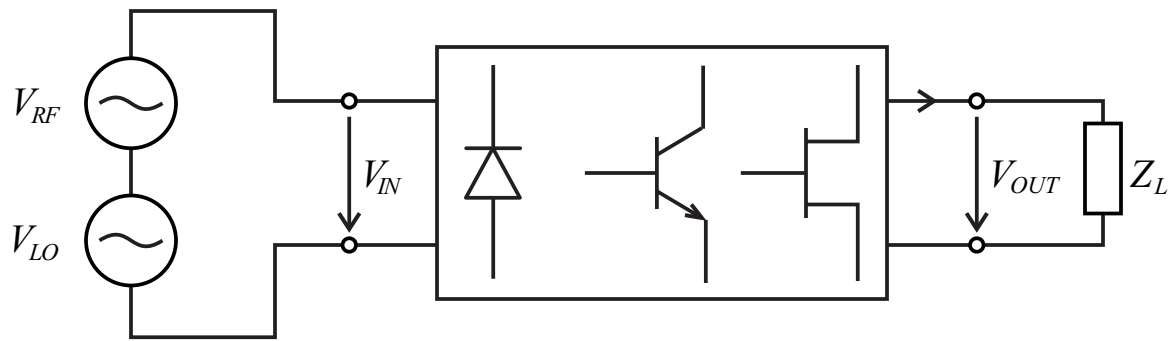
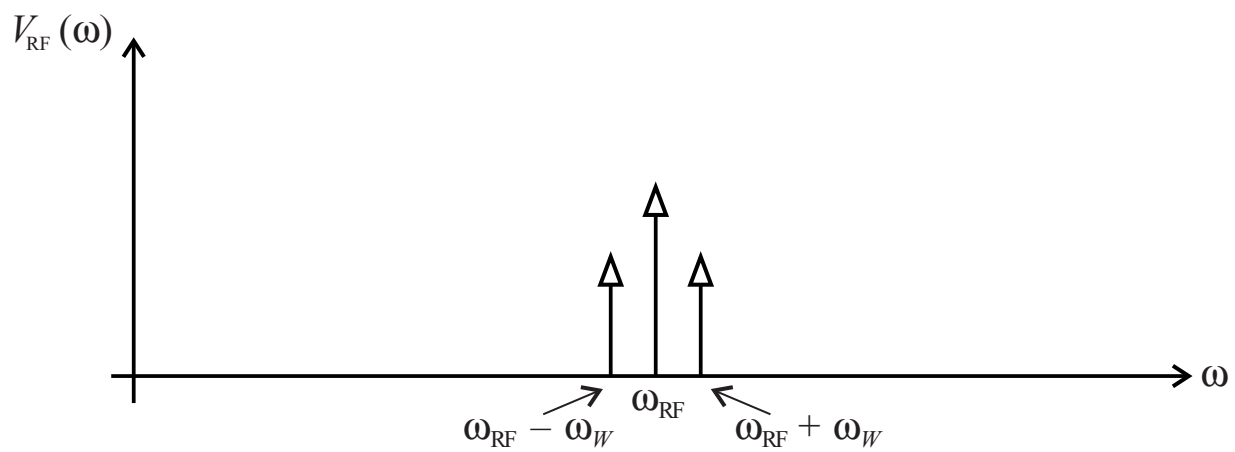
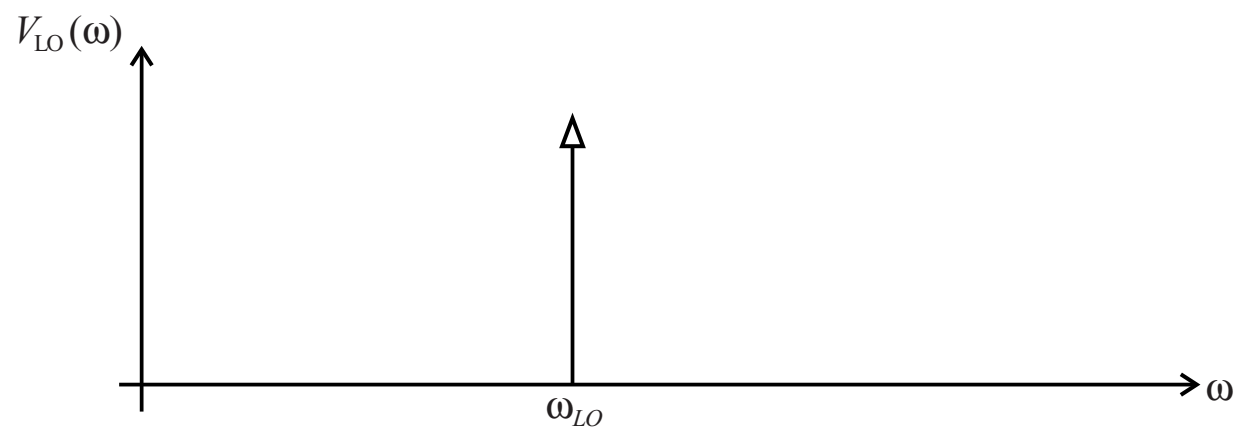


Figure 10-30 Basic mixer concept: two input frequencies are used to create new frequencies at the output of the system.



(a) RF signal



(b) LO signal



(c) Down- and upconverted spectral products

Figure 10-31 Spectral representation of mixing process.

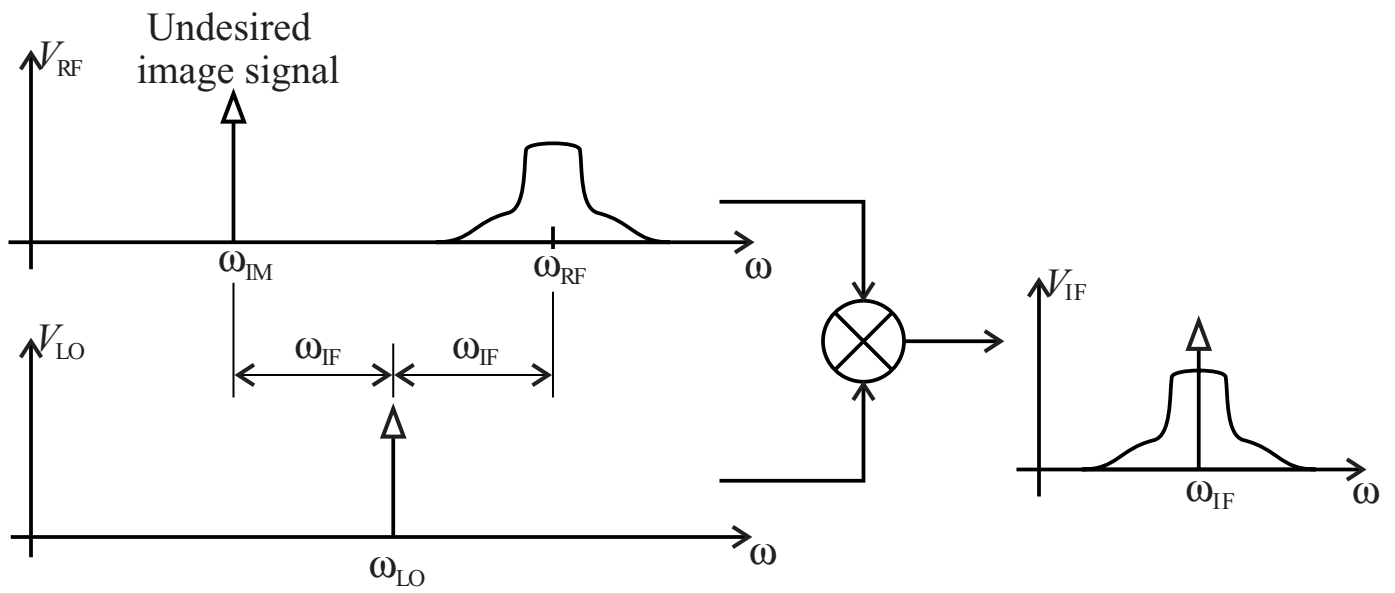
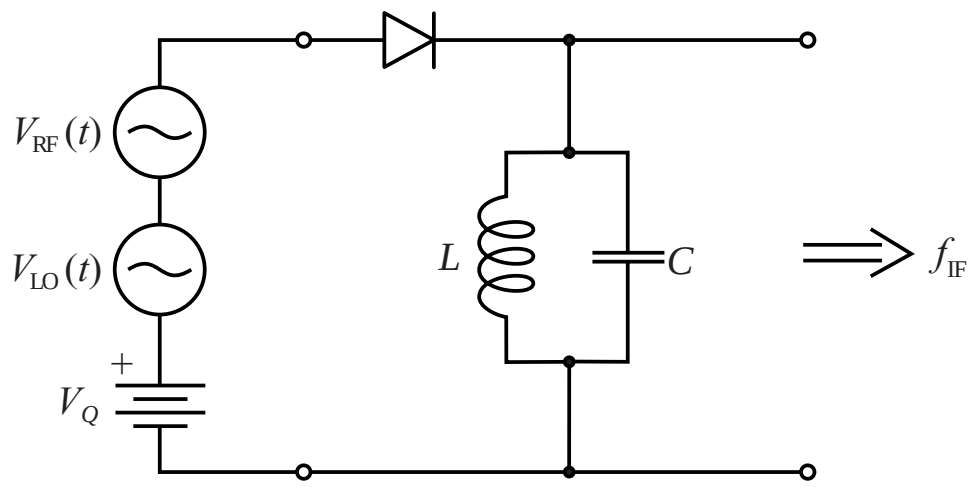
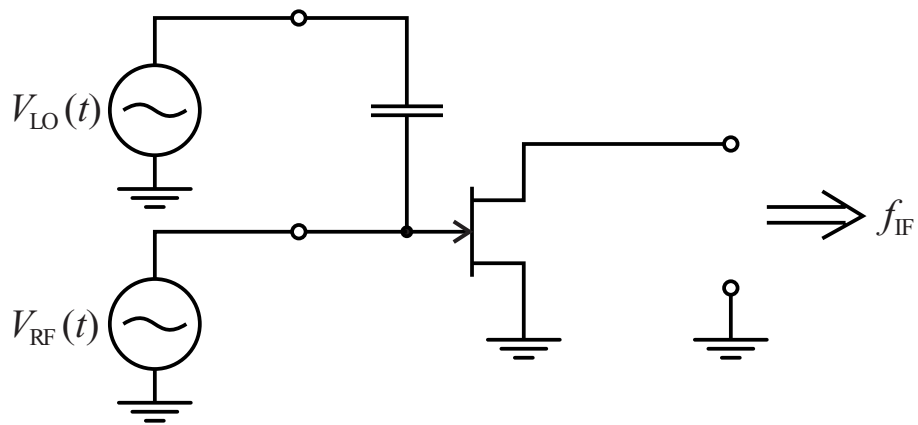


Figure 10-32 Problem of image frequency mapping.



(a) Diode mixer



(b) FET mixer

Figure 10-33 Two single-ended mixer types.

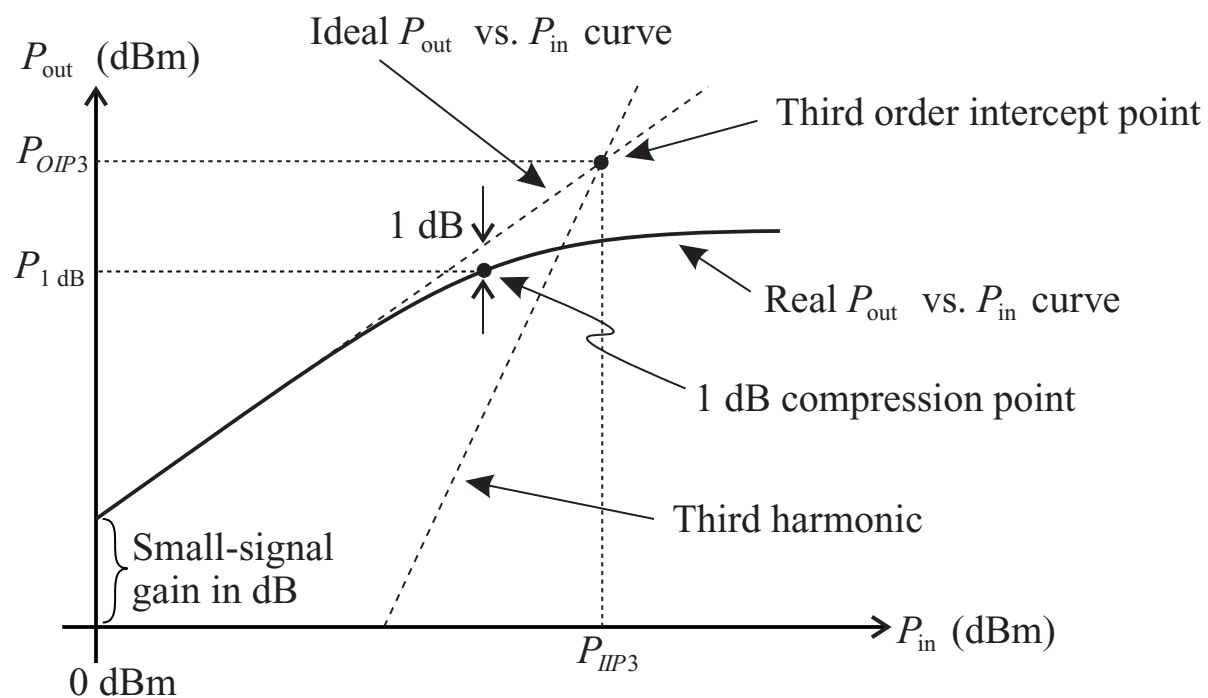


Figure 10-34 Conversion compression and intermodulation product of a mixer.

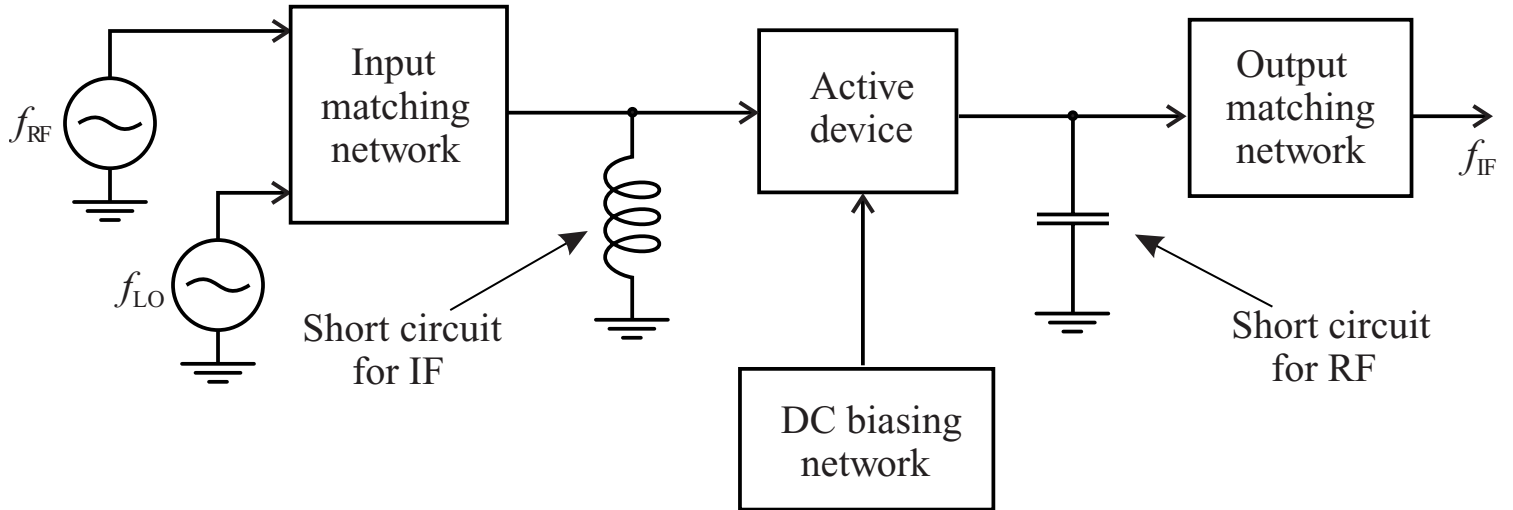


Figure 10-35 General single-ended mixer design approach.

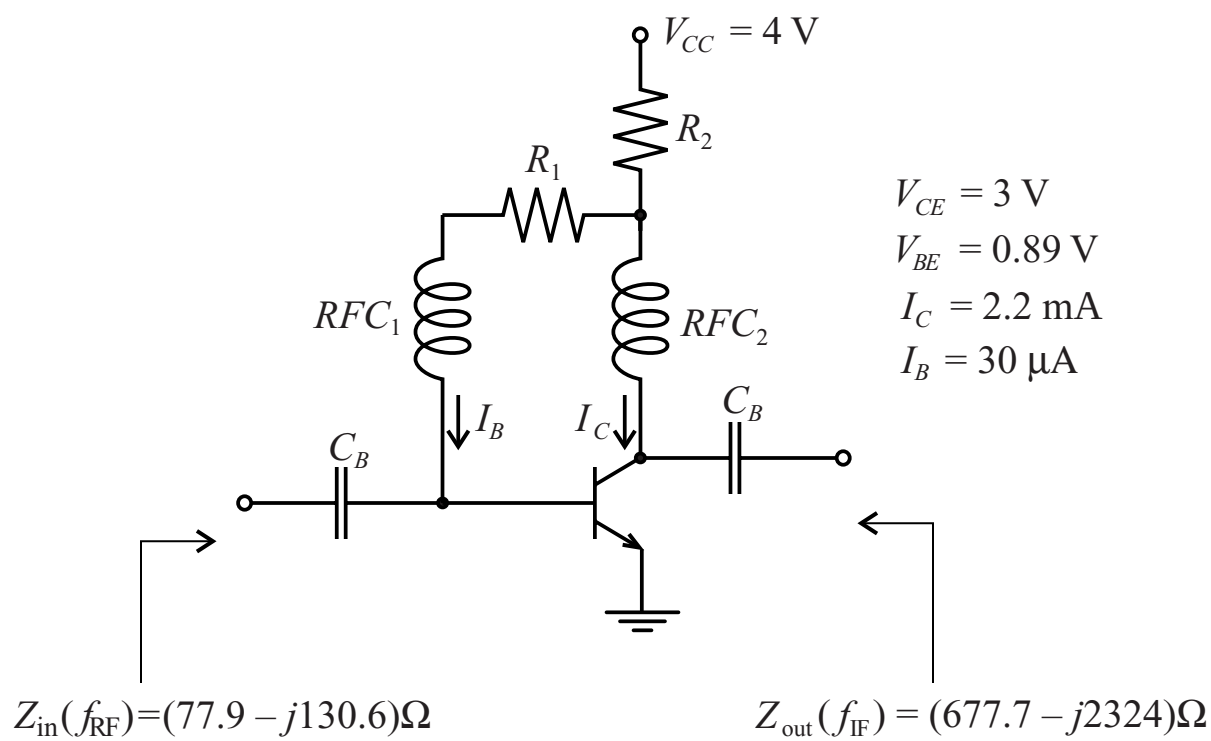


Figure 10-36 DC-biasing network for BJT mixer design.

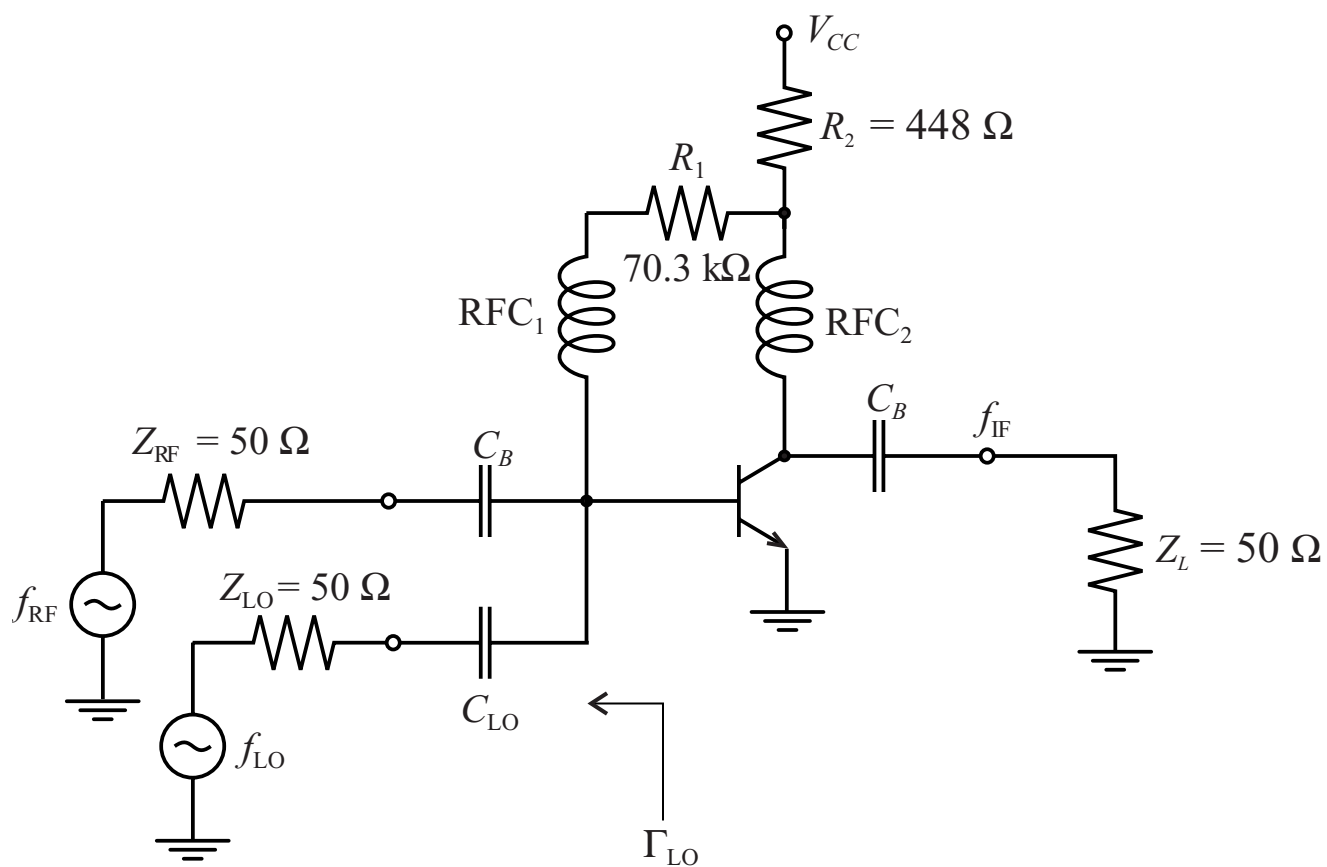


Figure 10-37 Connection of RF and LO sources to the BJT.

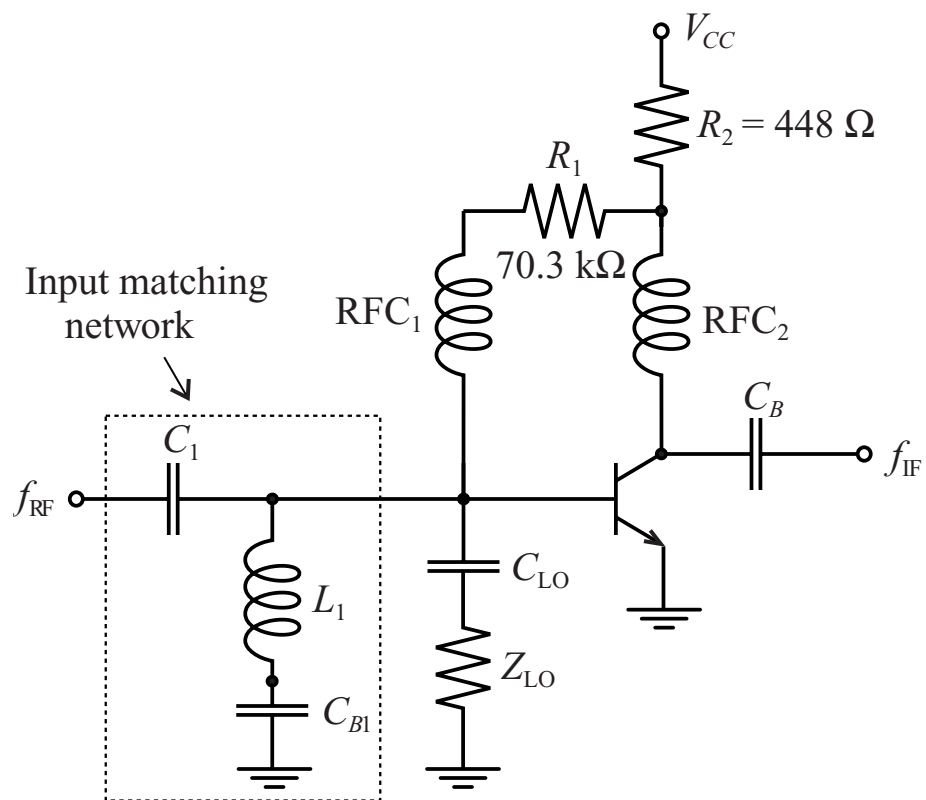


Figure 10-38 Input matching network for a single-ended BJT mixer.

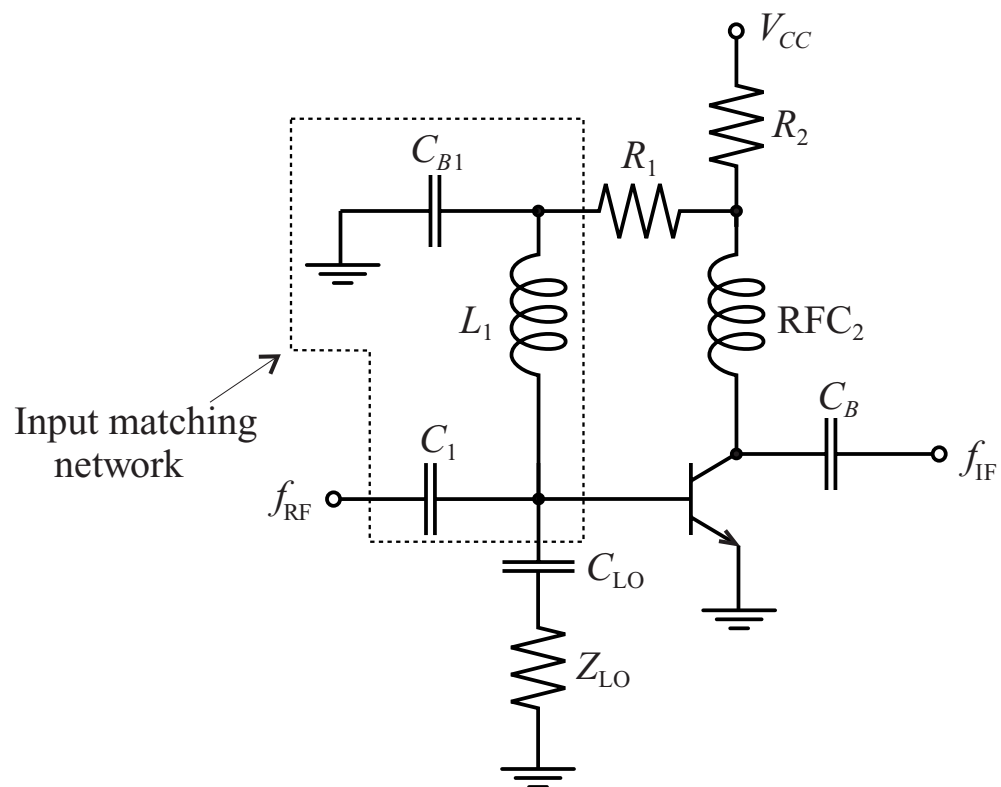


Figure 10-39 Modified input matching network.

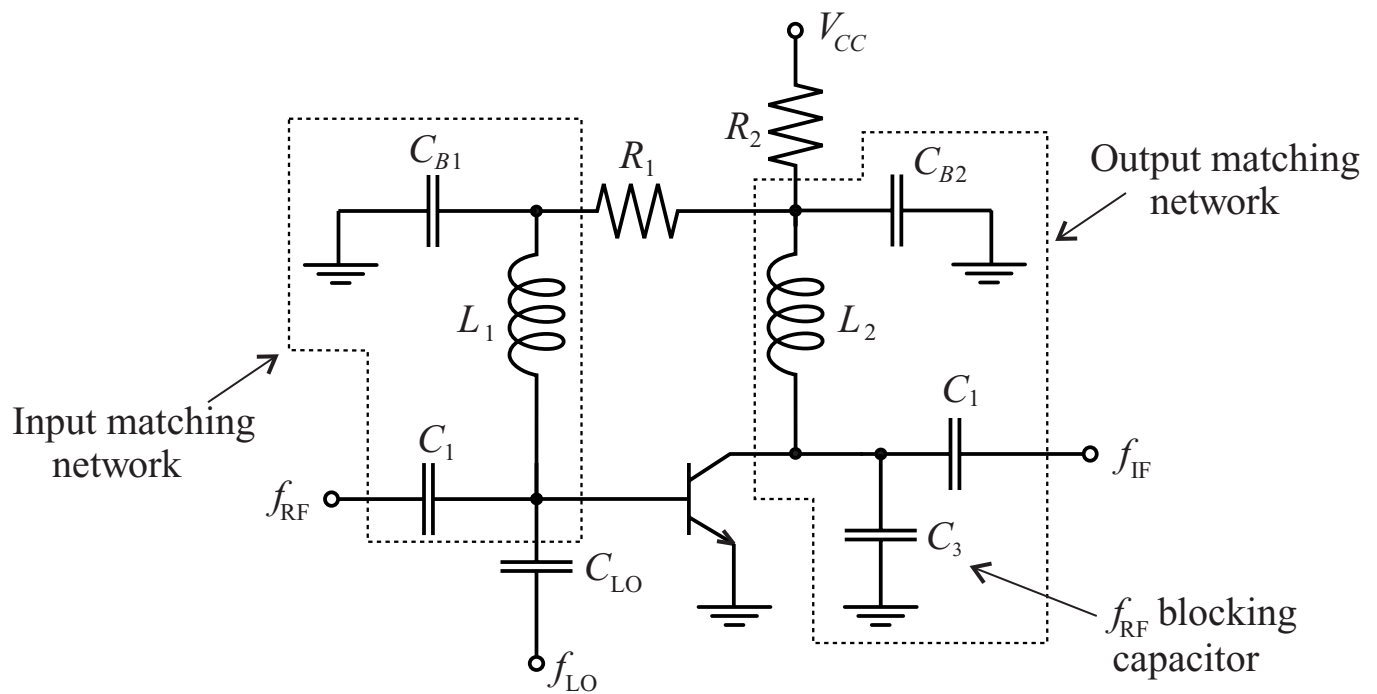


Figure 10-40 Complete electrical circuit of the low-side injection, single-ended BJT mixer with $f_{RF} = 1900$ MHz and $f_{IF} = 200$ MHz.

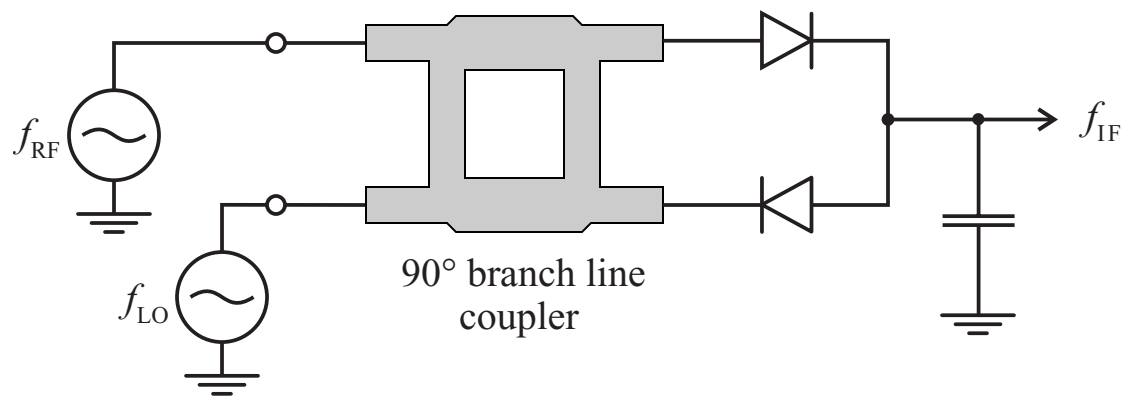


Figure 10-41 Balanced mixer involving a hybrid coupler.

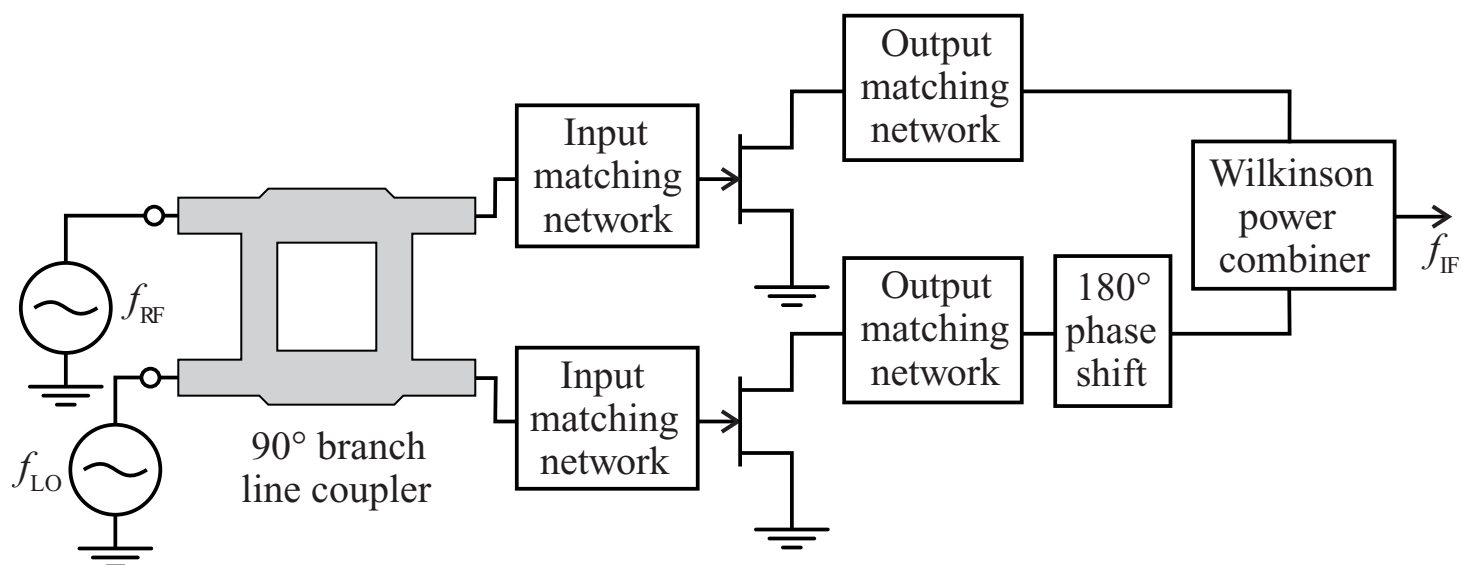


Figure 10-42 Single-balanced MESFET mixer with coupler and power combiner.

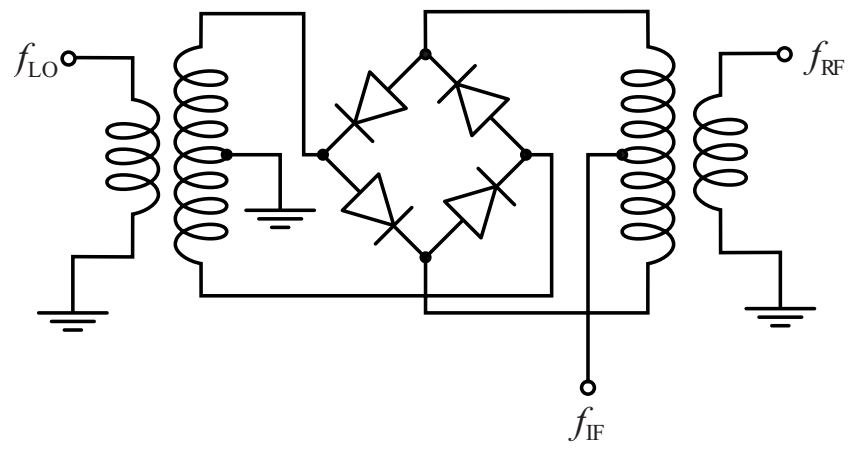


Figure 10-43 Double-balanced mixer design.